Application Report
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Interfacing Low Power Serial (SPI) ADCs to the MSP430F449

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Data Acquisition - Digital/Analog Converters

ABSTRACT

This application report discusses the serial peripheral interface (SPI) implementation of a data acquisition system featuring the following devices: TLV2541, TLC2551, TLC3541, and TLC4541. These analog-to-digital converters (ADC) offer options for users ranging from extremely low power and wide voltage supply range to fast conversion throughput. All devices share a small (MSOP) footprint and are pin-for-pin compatible for easy upgrading. In this application report, SPI interface code examples from the MSP430F449 to each ADC are presented. Using the TLV2541, TLC2551, TLC3541, or TLC4541 EVMs along with the HPA449 evaluation system from SoftBaugh™, makes developing the interface even easier.

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1 Introduction

The main features for the four ADCs in this family are shown in Table 1.

Table 1. Main Features of the Four ADCs

DEVICE	RESOLUTION (BITS)	SAMPLE RATE (KSPS)	SUPPLY (V)	POWER (mW)	DNL (LSB)	INL (LSB)
TLV2541	12	200	2.7 – 5.5	2.3	1	1
TLC2551	12	400	5	15	1	1
TLC3541	14	200	5	17.5	1	1
TLC4541	16	200	5	17.5	2	2.5

The TLV2541, TLC3541, and TLC4541 possess an internal conversion clock, which relieves the microprocessor or host system of providing a conversion clock. The TLC2551 does not possess an internal conversion clock; therefore, it is important that the microprocessor/host system generate the necessary clock signals to enable conversions to complete when using this device.

A summary of the most important details of each device in this family is given in Table 2.

Table 2. Summary of Important Details

DEVICE	SAMPLING	CONVERSION	RESET REQUIRED?	$\overline{CS}$ must be asserted LOW at least until
TLV2541	5th SCLK until 16th SCLK	3.5 µs	No	Conversion is complete
TLC2551	5th SCLK until 16th SCLK	28 SCLKs	No	Conversion is complete
TLC3541	5th SCLK until 24th SCLK	2.67 µs	Yes	Sampling is complete
TLC4541	5th SCLK until 24th SCLK	2.94 µs	Yes	Sampling is complete

These devices are available in two package styles, SOIC (small outline integrated circuit) or MSOP (micro small outline package). Data sheets, pinouts, and package details are available at http://www.ti.com.

2 Hardware Setup Configuration

As indicated in Table 2, the software must address certain requirements in order to properly satisfy the ADC's hardware. These hardware needs are examined in this section.

This application report is based on using the HPA449 platform for the MSP430F449 and any of these ADC EVMs: TLV2541, TLC2551, TLC3541, and TLC4541. The HPA449 evaluation system is available from SoftBaugh, Inc. (http://www.softbaugh.com). Once the HPA449 and any of the EVMs are configured properly, they can easily be connected. Figure 1 shows the hardware configuration setup for the HPA449 board.

The HPA449 comes from the factory configured with the correct jumper settings (see Figure 1). See the HPA449 user's guide. J19 should be removed to separate LED D2 from the P3.7 output (which is the $\overline{CS}$ control for the ADCs in this application). LED D1 is used to flash on and off on the HPA449 board when all the samples have been taken.

Evaluation modules for the TLV2541, TLC2551, TLC3541, and TLC4541 are available from Texas Instruments. The modules contain all the necessary support circuitry to evaluate ADC performance and begin development work. Figure 2 shows the outline of a typical module. The only requirement for the ADC EVMs setup is that the **FS** of the ADC EVM be tied high (to VDD). This can be done by removing jumper W4 and tying pin 3 (+5V) of W6 to pin 2 of W4. The ADC EVM then is plugged into Serial Site A of the HPA449 board (as shown on Figure 1).

Port 3 of the MSP430F449 can be either general digital I/O or can be configured for UART (universal asynchronous/synchronous receive/transmit) operation. The diagram in Figure 3 indicates the relevant pins for ADC connection to the MSP430F449.

The MSP430F449 microcontroller interfaces with the ADC using the SPI serial data communication protocol via the MSP430 microcontroller's USART0 port. Only two pins of the four-pin SPI mode of configuration are used (UCLK0 and SOMI0). This implementation makes it unnecessary to write any data to the ADC because only the digital data from the converter is read into 500 memory spaces within the MSP430 memory. The $\overline{CS}$ is controlled by pin 3.7 of the MSP430 set as a GPIO output. Therefore, the STE and the MISO functions in SPI mode of the USART0 port are not used. See Figure 3.

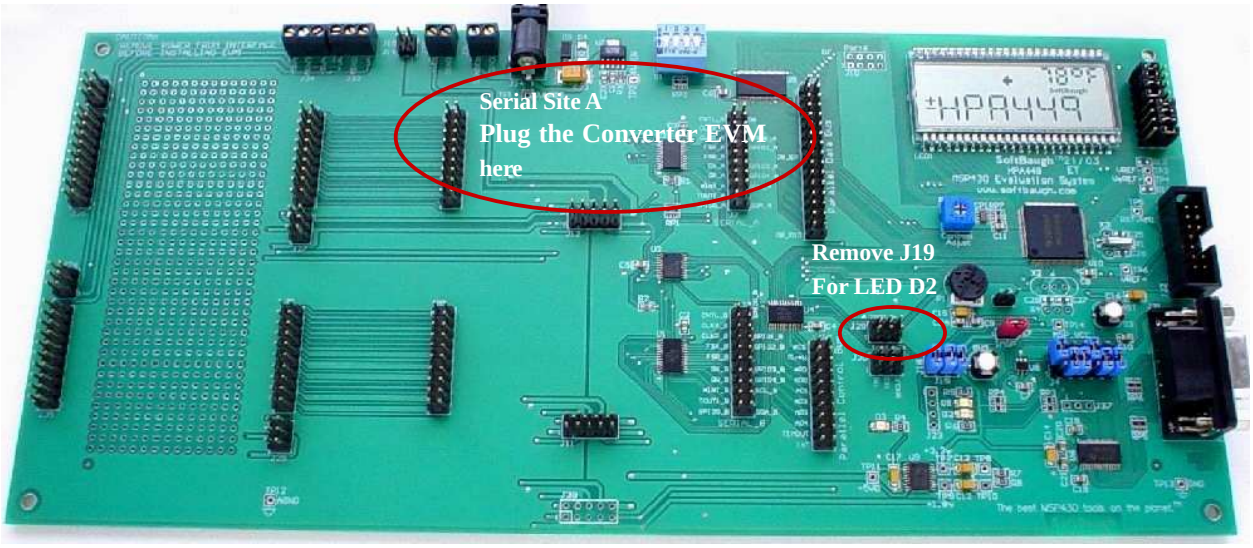

Figure 1. HPA449 Board From SoftBaugh

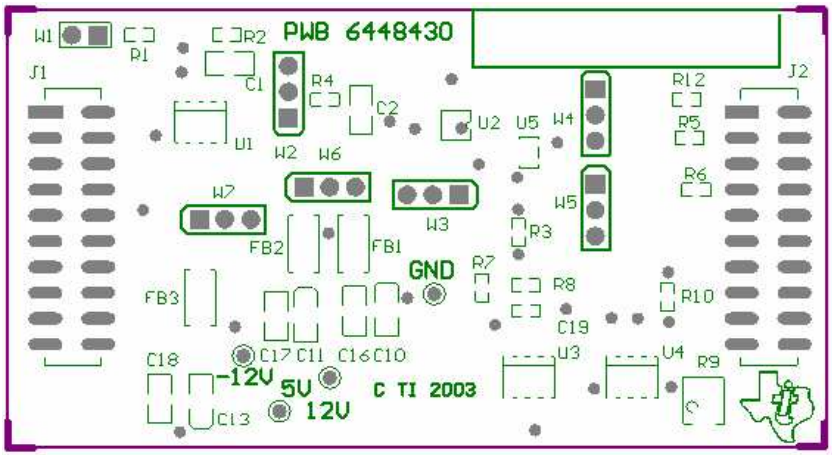

Figure 2. ADC EVM Board Layout

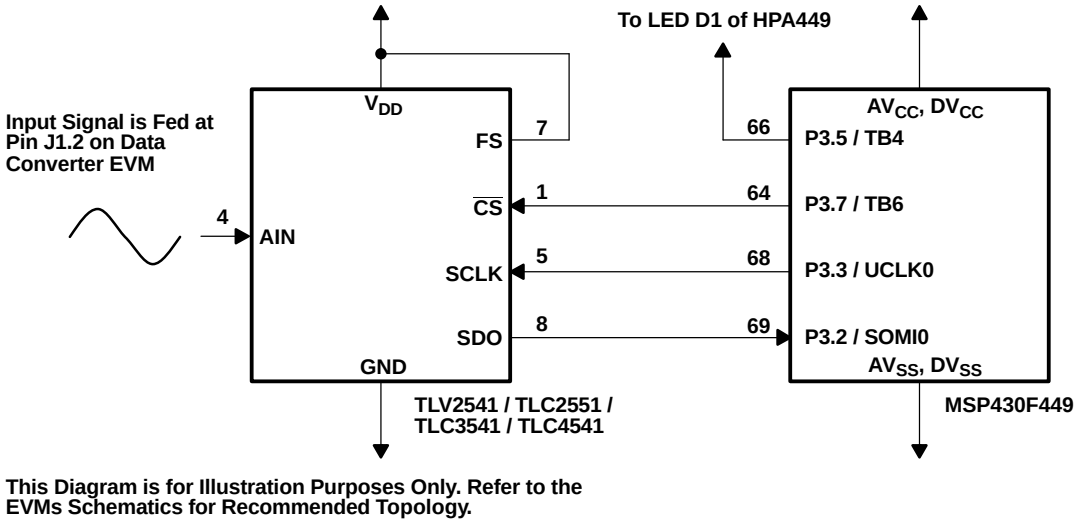

Figure 3. MSP430 Hardware I/O

2.1 Reset

The TLV2541 and TLC2551 do not require a reset cycle; however, the TLC3541 and TLC4541 ADCs do. The first word of data after a valid reset cycle is given in Table 3.

Table 3. Data After Valid Reset Cycle

DEVICE	DATA AFTER VALID RESET CYCLE
TLC3541	3FC0 (hex)
TLC4541	FF00 (hex)

It is useful to confirm that the ADC has been reset properly, prior to reading any converted data. Figure 4 shows an example of a valid reset. In this condition, $\overline{CS}$ is asserted low for more than four SCLKs and less than eight SCLKs.

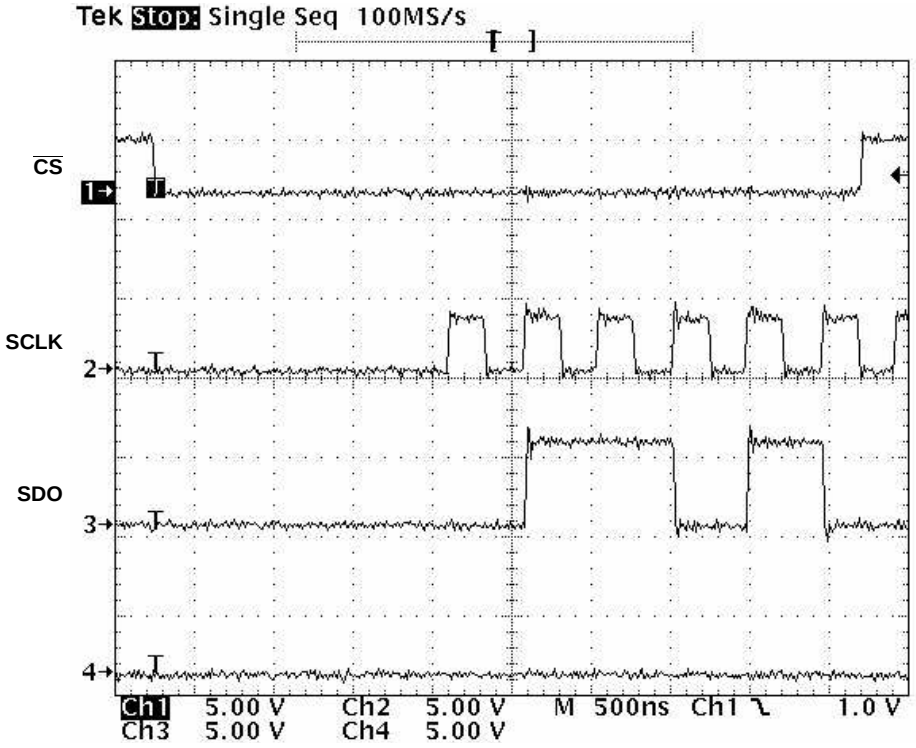

Figure 4. Valid Reset Cycle – TLC3541/TLC4541

2.2 Sampling Process

The sample process begins after the first 5th SCLK transition. The conversion process is initiated automatically after the sample has been completed.

The number of SCLKs required for successful sampling for each device is given in Table 4.

Table 4. SCLKs for Sampling

DEVICE	SCLKs for SAMPLING
TLV2541	12 SCLKs
TLC2551	12 SCLKs
TLC3541	20 SCLKs
TLC4541	20 SCLKs

The most important point that the user should note during sampling is that $\overline{CS}$ remains asserted low during the process. If $\overline{CS}$ is de-asserted prematurely, the process is invalid.

2.3 TLV2541, TLC3541, and TLC4541 Conversion Process

Because the TLV2541, TLC3541, and TLC4541 have an internal oscillator, it is not necessary to provide any extra SCLKs for conversion.

For each device, conversion proceeds as shown in Table 5.

Table 5. Device and Conversion

DEVICE	CONVERSION BEGINS AFTER	CONVERSION TIME	CONVERSION ERROR
TLV2541	16 SCLKs	3.5 µs maximum	No indication
TLC3541	24 SCLKs	2.67 µs maximum	3FC0 (h)
TLC4541	24 SCLKs	2.94 µs maximum	FF00 (h)

For the TLV2541, $\overline{CS}$ should remain asserted low during the conversion process.

For the TLC3541 and TLC4541, $\overline{CS}$ can be de-asserted high during conversion. If $\overline{CS}$ is de-asserted high and then asserted low without giving the ADC enough time to complete the conversion, these devices will output the reset code previously discussed, to indicate that there was an error.

Figure 5, Figure 6, and Figure 7 detail the process involved in achieving successful conversions with each of these devices. Note that the SDO data that is present on Figure 5 during the conversion is the output data from the previous conversion.

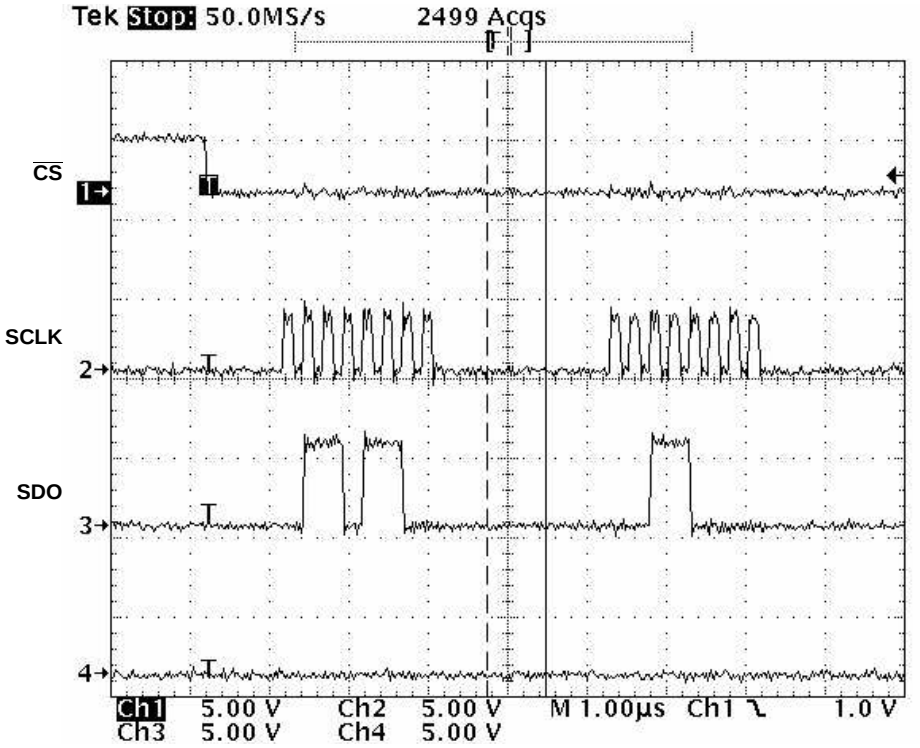

Figure 5. TLV2541 Conversion Process

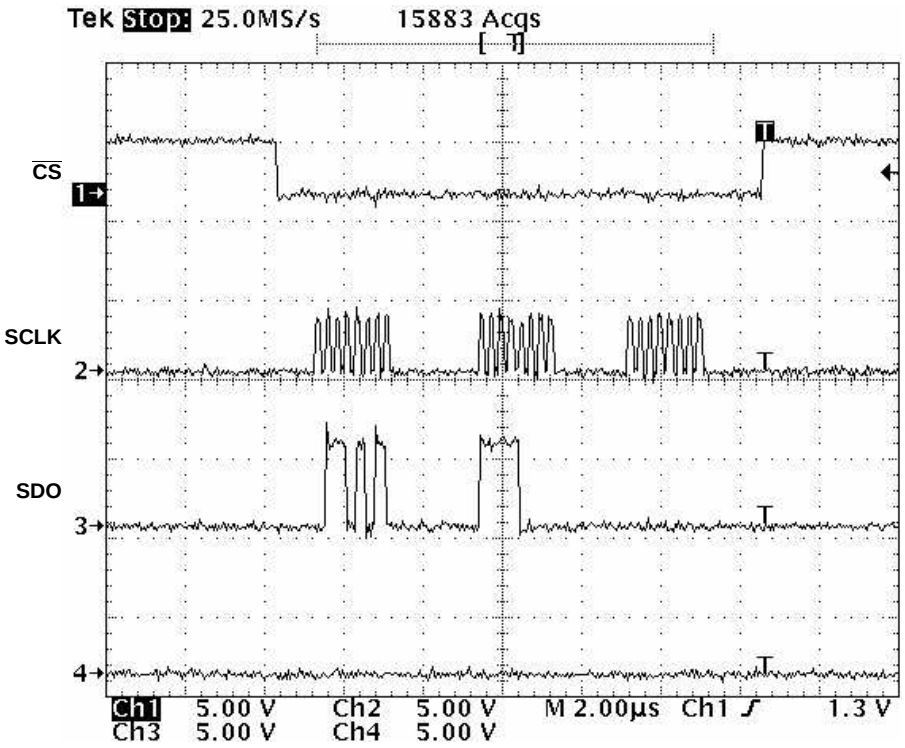

Figure 6. TLC3541 Conversion Process

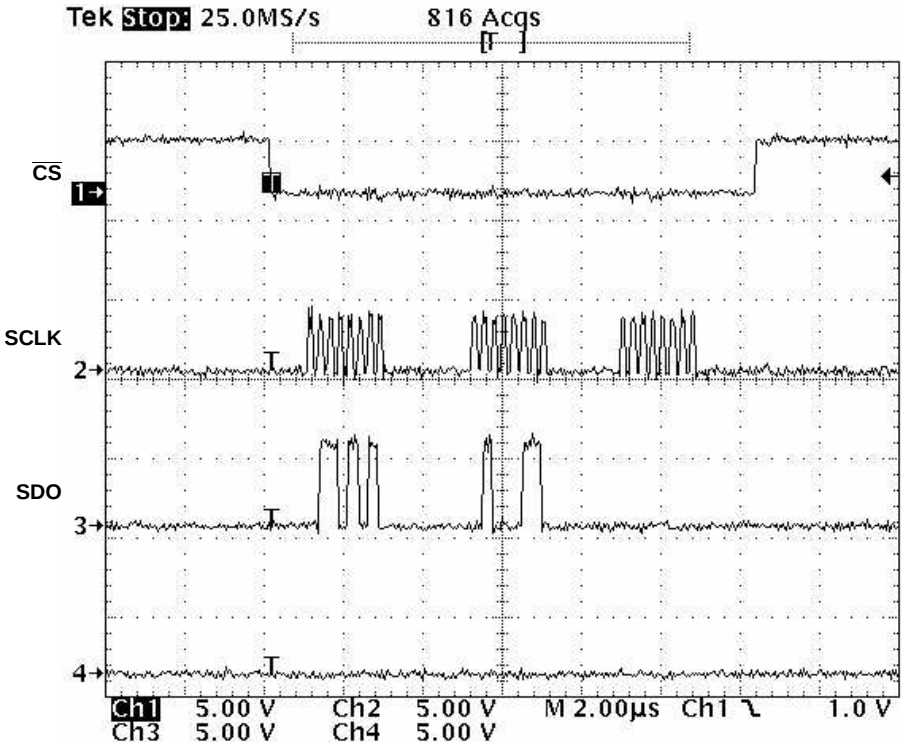

Figure 7. TLC4541 Conversion Process

2.3.1 TLC2551 Conversion Process

Following sampling, the conversion is complete after the required number of conversion clocks. Because the TLC2551 does not possess an internal conversion oscillator, the device uses SCLK as the conversion clock and relies on the user to transmit at least 28 SCLKs. In regular SPI operation, SCLK is generated and transmitted by the microcontroller in packets of eight at a time. This means that by default the user transmits 32 SCLKs (4×8) to provide sufficient conversion clocks. During this time, $\overline{CS}$ should remain asserted low.

Following the transfer of four packets of SCLKs, $\overline{CS}$ should be de-asserted high. See Figure 8 for details.

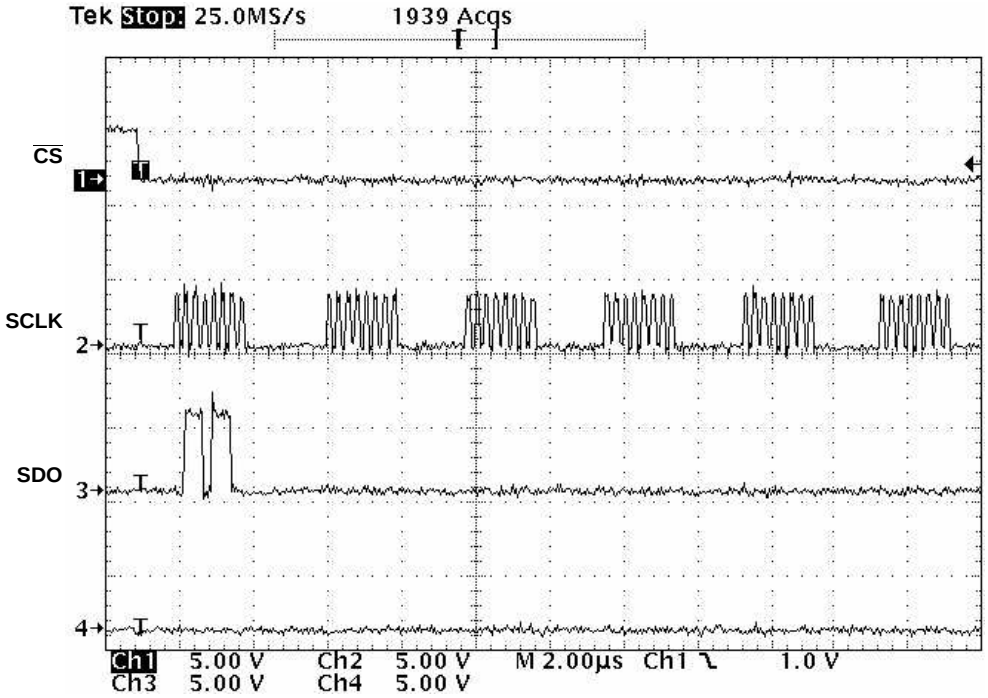

Figure 8. TLC2551 Conversion Process

2.4 Data Transfer

For all the devices discussed, the transfer of data to the microcontroller occurs following the low assertion of $\overline{CS}$ and progresses bit-by-bit, beginning with the most significant bit (MSB), on successive falling edges of SCLK.

The TLV2541 and TLC2551 require at least one falling clock edge while $\overline{CS}$ is de-asserted high to enable data output on the next cycle. Each cycle may be started by $\overline{CS}$, FS, or a combination of both (only $\overline{CS}$ is used in this application report). The internal state machine requires one SCLK high-to-low transition to determine the state of these control signals so that internal blocks can be powered up in an active cycle. For simplicity, to make sure that there is at least one SCLK transition whenever $\overline{CS}$ is de-asserted high, the included software simply sends eight extra bits (or a dummy transmission). Customers in their applications can also opt to simply toggle the SCLK pin once.

The TLC3541 and TLC4541 do not have these requirements.

3 Software Development

The software for the ADCs was developed using TI's integrated development environment (IDE) for the MSP430 (IAR embedded workbench, Kickstart version).

3.1 Software Overview

A detailed description of the software is beyond the scope of this application report. Figure 9 shows an overview of the process, briefly described as follows:

- MSP430F449 setup occurs—including any GPIO pins that must perform special functions, and assigning UART0 as the SPI port.
- Following setup, if the ADCs are the TLC3541 or TLC4541, the ADC is reset as previously described. Care should be taken at this point to ensure that the $\overline{CS}$ signal is more than four SCLKs and less than eight SCLKs. Trial and error is involved because the duration of $\overline{CS}$ is related to the SCLK frequency—therefore, if the SCLK frequency changes, the $\overline{CS}$ duration may have to be altered. For the TLV2541 and TLC2551, a reset cycle is not required.
- The software takes 512 samples from AIN0, storing them in an array named adc_data.
- The HPA449 board does not include an 8-MHz resonator, but the customer can install one if desired. The software allows the application to run without the resonator by simply defining the resonator as (0) in the #define choice. A (1) should be selected if the resonator is installed.
- The C program is written to be able to program any of the following EVMs: TLV2541, TLC2551, TLC3541, and TLC4541. By choosing the appropriate #define statement for the EVM board being used (by assigning a 1 to it), and de-selecting the other three boards (by assigning a 0 to the others), the program is flexible for working with all the boards mentioned, one at a time.

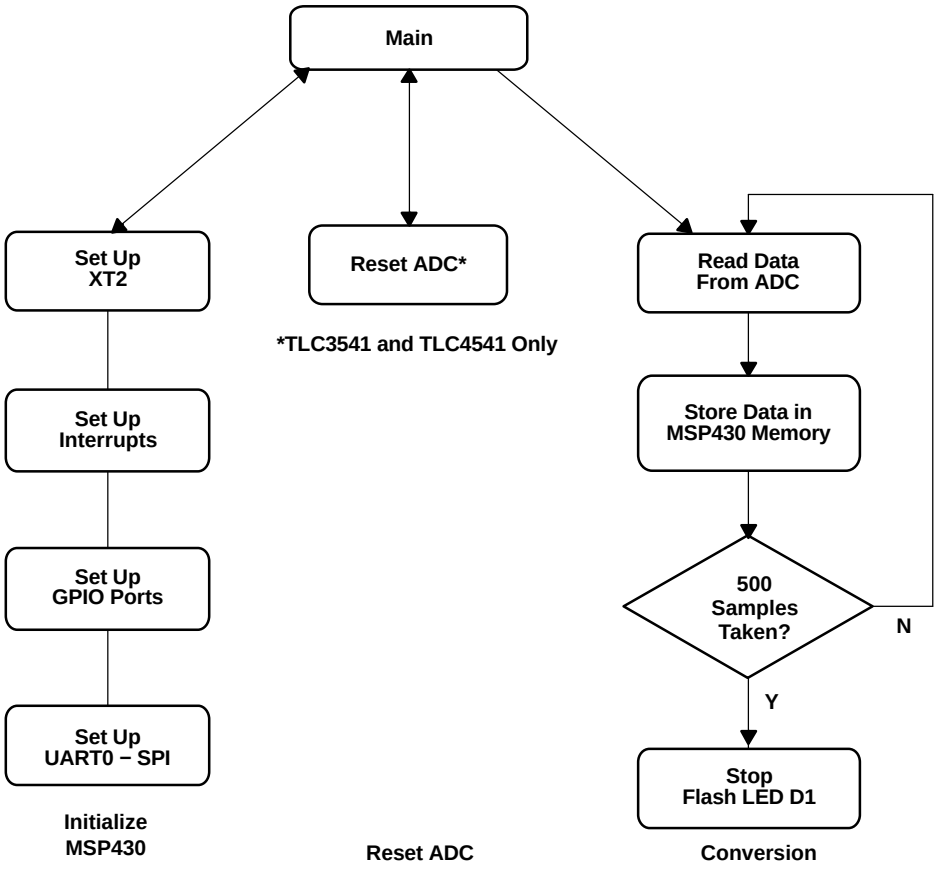

Figure 9. Software Overview

4 References

1. *TLV2541, 2.7-V to 5.5-V, Low-Power, 12-Bit, 140/200 KSPS, Serial ADC with Autopower Down* data sheet (SLAS245)
2. *TLC2551, 5-V, Low-Power, 12-Bit, 175/360 KSPS, Serial ADC with Autopower Down* data sheet (SLAS276)

3. *TLC3541, 5-V, Low Power, 14-Bit, 200-KSPS, Serial ADC with Auto-Power Down* data sheet (SLAS345)
4. *TLC4541, 5-V, Low Power, 16-Bit, 200-KSPS, Serial ADC with Auto-Power Down* data sheet (SLAS293)
5. *TLV2541, TLC2551, TLC3541, and TLC4541 EVM User's Guide* (SLAU103)
6. *MSP430F449 Mixed Signal Microcontroller* data sheet (SLAS344)
7. MSP430F44X Evaluation System (HPA449) User's Guide (SoftBaugh, Inc.)
8. *MSP430F44X Family User's Guide* (SLAU056)

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