

# **Interfacing the TLC4541 and the DAC7654 to the MSP430F449**

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*Data Acquisition - Digital/Analog Converters*

## **ABSTRACT**

The purpose of this application report is to demonstrate the combination of a serial analog-to-digital converter (ADC) and a serial digital-to-analog converter (DAC) on a development platform. The ADC and the DAC featured are the TLC4541 and the DAC7654, respectively. These devices are presented using the HPA449 as a low-cost development platform. The application report briefly describes each component and presents a software example in which the analog input signal is digitized; the digital data is read by the HPA449 before finally being written to the DAC for inspection of the regenerated signal.

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## 1 Introduction

The main features of the TLC4541 and DAC7654 are shown on [Table 1](#).

**Table 1. Main Features of the TLC4541 and DAC7654**

PARAMETER	TLC4541	DAC7654
Resolution (bits)	16	16
Sample Rate (max)	200 KSPS	–
Settling Time ( $\mu$ s)	–	12
Architecture	SAR	R-2R
Number of Input Channels	1	–
Number of Output Channels	–	4
Input Type	Voltage	–
Output Type	–	Voltage
Supply (V)	5	5
Power (mW)	17.5	18
DNL ( $\pm$ LSB)	2	1
INL ( $\pm$ LSB)	2.5	3
Interface	Serial, SPI	Serial, SPI

The 16-bit TLC4541 is a high-performance, low-power, miniature CMOS ADC. This device operates from a single 5-V supply. It is designed to operate with low power consumption. The power-saving features are further enhanced with an auto-power-down mode. The device uses a built-in oscillator as the conversion clock, providing a 2.94- $\mu$ s maximum conversion time.

The DAC7654 is a quad voltage output DAC with 16-bit monotonic performance over the specified temperature range. The DAC7654 can operate from a single +5-V supply or from +5-V and –5-V supplies. It is also a low-power device, featuring a double-buffered DAC input (allowing simultaneous update of all DACs), and provides a serial data output for daisy-chaining multiple DACs. Another useful feature is the Programmable Asynchronous Reset which clears all registers to a midscale code of 8000h or to a zero-scale of 0000h.

Both of these devices were chosen for this application report due to their various similarities (number of bits, low power, input/output type, supply voltage, etc.) and because both have the capability of direct 3-wire interface to the serial port of most popular host microprocessors (SPI interface).

## 2 Hardware Setup Configuration

Certain requirements must be addressed in order to properly satisfy the ADC and the DAC hardware. These hardware needs are examined in this section.

### 2.1 HPA449 Board

This application report is based on using the HPA449 platform from SoftBaugh™, Inc. which incorporates an MSP430F449 microprocessor. Both the TLC4541EVM and the DAC7654EVM are installed onto the appropriate sites, as shown in [Figure 1](#).

The HPA449 is factory configured with the default jumper settings used in this application report (see [Figure 1](#)); [Table 2](#) indicates only those jumpers that should be changed from the default position. See the HPA449 User's Guide for details about the board and the default jumper settings (<http://www.softbaugh.com>).

LED D1 flashes when the system is operating correctly. If the ADC does not reset properly, LED D1 remains on, indicating that the program has stopped running.

The signal driving LED D2 is P3.7; this pin is also used by the MSP430 as  $\overline{CS}$  for the ADC. Therefore, the shunt at J19 should be removed to disconnect this pin from the LED and allow it to act as  $\overline{CS}$  only. For the DAC operation, the only requirement is to add another jumper on J30 pins 3 and 4 to route the correct signal for the RSTSEL pin function of the DAC7654EVM.

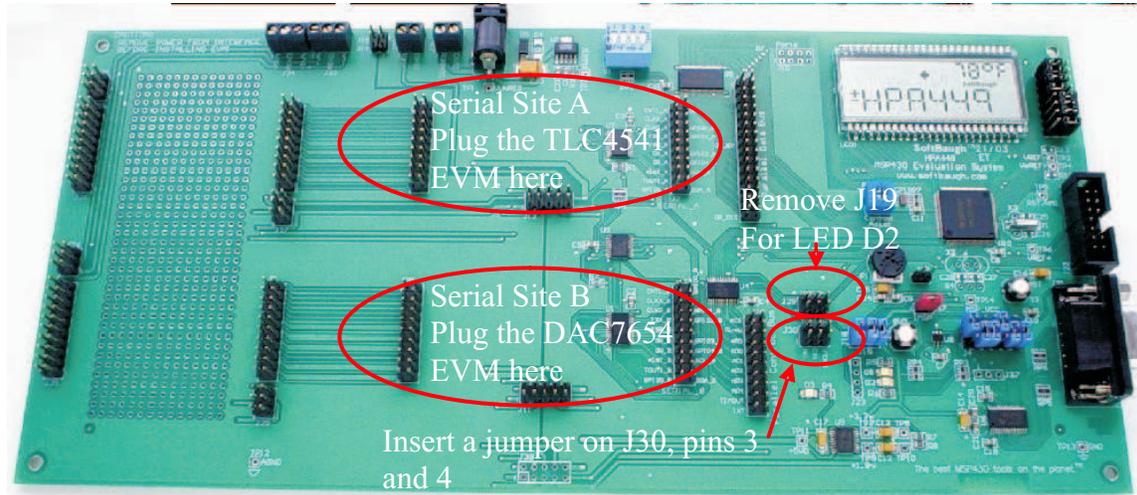


Figure 1. HPA449 Board From SoftBaugh

Table 2. Non-Default Setting of Jumpers for the HPA449 Board

DESIGNATOR	JUMPER POSITION			FUNCTION
	1-2	3-4	5-6	
J19	OPEN	–	–	Jumper to connect D2 to MSP430 P3.7
J30	OPEN	CLOSED	OPEN	TOUTB Selector

## 2.2 TLC4541EVM

The TLC4541EVM contains all the necessary support circuitry to evaluate the ADC's performance and begin development work. The EVM is shown in Figure 2 and is shipped with a factory-set jumper configuration; Table 3 indicates only those jumpers that should be changed from the default position in order to ensure that the FS pin of the ADC is tied high to  $V_{DD}$  (by linking from pin 2 of W4 to pin 3 of W6). See the TLC4541EVM User's Guide (SLAU103) for information about the features, default jumper settings, board layout, bill of materials (BOM), and the schematic diagram.

Figure 3 shows a simplified diagram of the connections between the TLC4541 and the MSP430F449.

### 2.2.1 Analog Input

The analog input to the TLC4541 is via connector J1, pin 2 on the EVM (J1.2). See the ADC data sheets for the recommended magnitude of the analog input voltage.

### 2.2.2 Digital I/O

The MSP430F449 microcontroller interfaces with the ADC using the SPI serial data communication protocol via the MSP430 microcontroller's USART0 port. (Selected pins of port 3 of the MSP430F449 are configured for universal synchronous/asynchronous receive/transmit, or UART operation). Only two pins of the four-pin SPI mode of configuration are used (UCLK0 and SOMI0). This implementation makes it unnecessary to write any data to the ADC because only the digital data is being read from the converter into a couple of memory spaces (variables) that are then used by the DAC7654 DAC to output the same analog value. The  $\overline{CS}$  is controlled by pin 3.7 of the MSP430, set as a GPIO output. Therefore, the STE and the MISO functions in SPI mode of the USART0 port are not used. See Figure 3.

Hardware Setup Configuration

In this application,  $\overline{CS}$  enables and disables the serial communication (control via  $\overline{CS}$ , SPI interface). SPI mode is configured for CPOL = 0 and CKPH = 0

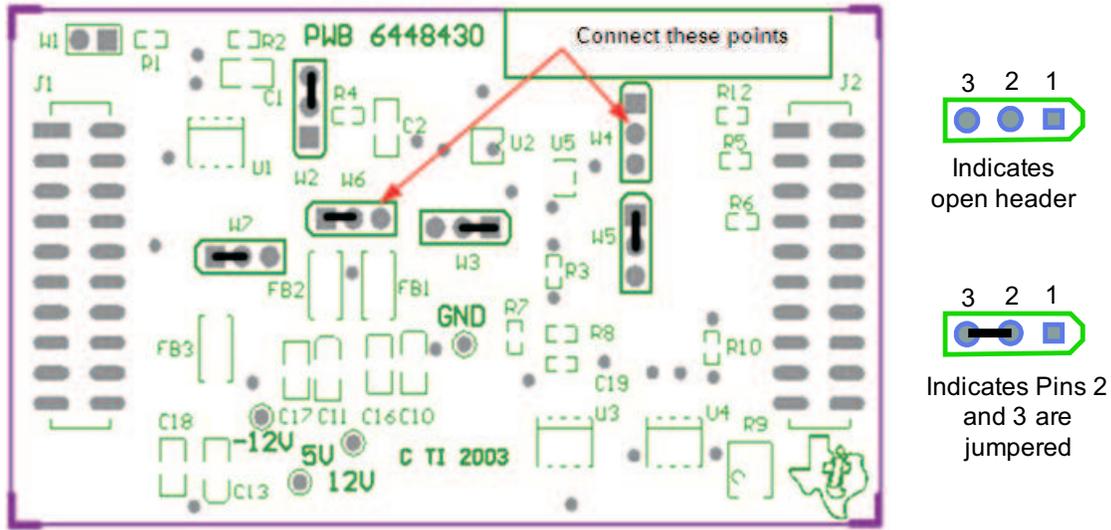
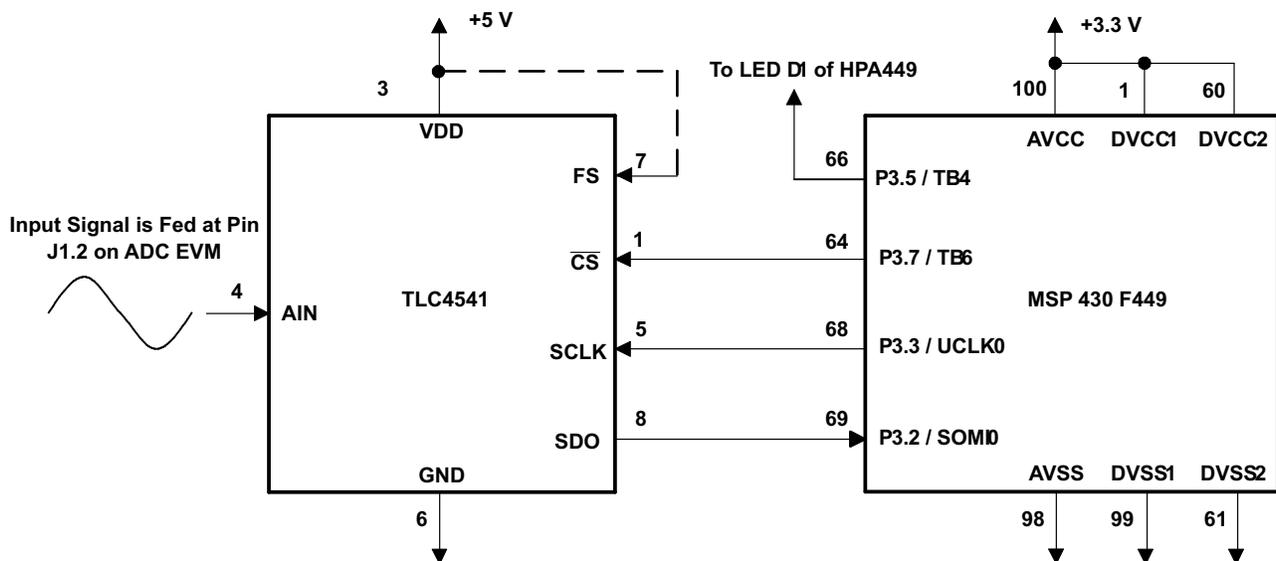


Figure 2. TLC4541EVM Hardware Configuration

Table 3. Non-Default Setting of Jumpers for TLC4541EVM Board

DESIGNATOR	JUMPER POSITION		FUNCTION
	1-2	2-3	
W4	OPEN	OPEN	FS of the ADC EVM tied high to VDD.
W6	CLOSED	OPEN	Note: This is accomplished by connecting pin 2 of W4 to pin 3 of W6.



NOTE: This diagram is for illustration purposes only. See the EVM schematic for recommended topology.

Figure 3. TLC4541 and MSP430F449 Hardware I/O

## 2.3 DAC7654EVM

The DAC7654EVM module contains all the necessary support circuitry to evaluate the DAC performance and begin development work (see [Figure 4](#) for the outline of a typical module). The module is factory configured with the default jumper settings, and [Table 4](#) shows the only jumpers that need to be changed to satisfy the requirements for the DAC EVM setup. See the DAC7654EVM User's Guide ([SLAU130](#)) for information about the features, default jumper settings, board layout, bill of materials (BOM), and the schematic diagram.

[Figure 5](#) shows the simplified schematic of how the DAC7654 and the MSP430F449 are interfaced with each other and indicates all the relevant pins for their connection.

### 2.3.1 Digital Input

The MSP430F449 microcontroller interfaces with the DAC7654 using the SPI serial data communication protocol via the MSP430F449 USART1 port. (Selected pins of port 4 of the MSP430F449 are configured for UART operation.) Only two pins are used out of the four-pin SPI mode of configuration. It is implemented this way because it is unnecessary to read any data back from the DAC7654. Therefore, the STE and the MISO functions in SPI mode of the USART1 port are not used.

In this application, the  $\overline{CS}$  enables and disables the serial communication (control via  $\overline{CS}$ , SPI interface). The SPI mode is configured for CPOL = 1 and CKPH = 0.

### 2.3.2 Analog Output

The analog output of the DAC7654EVM can be monitored at TP5 of the EVM.

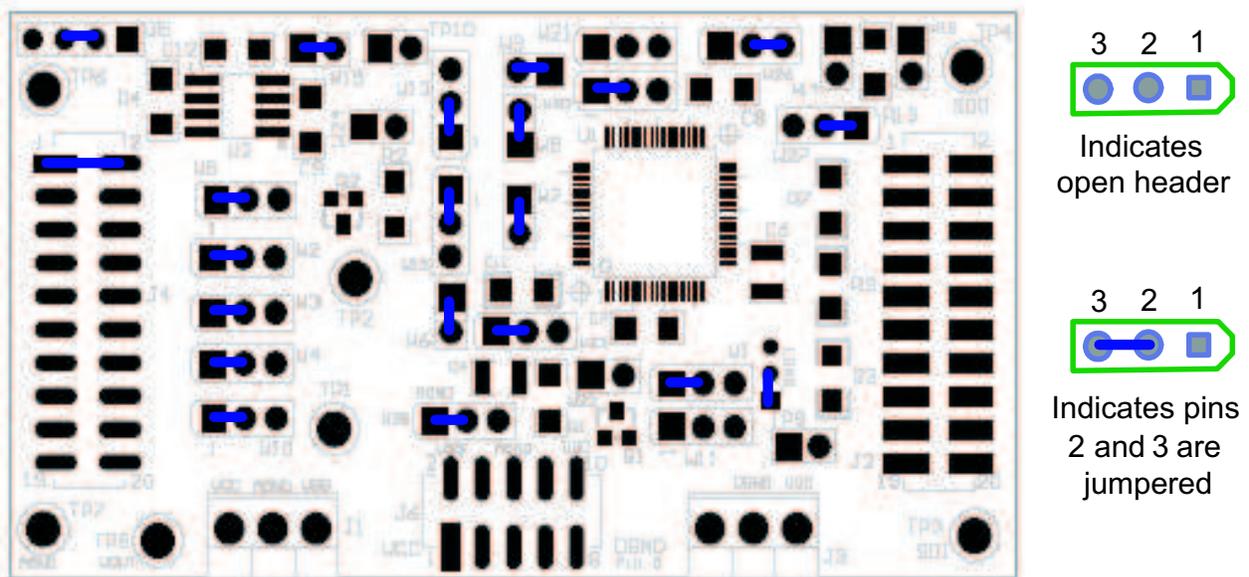


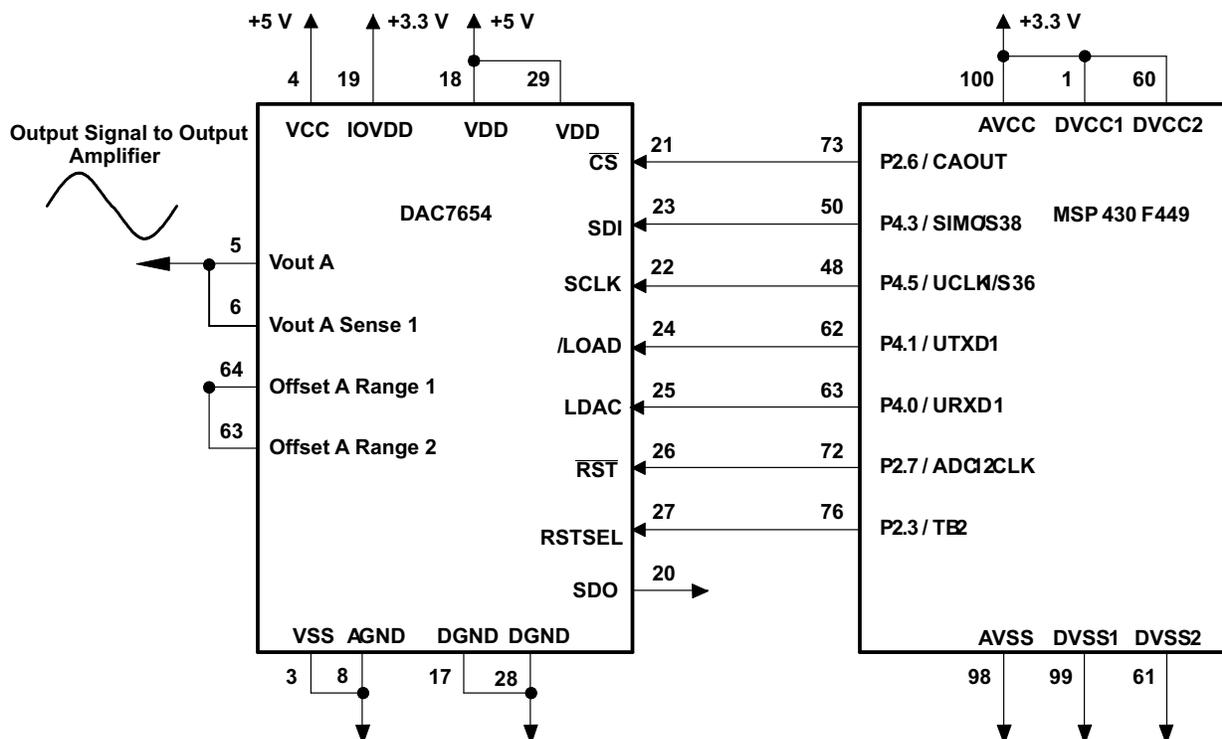
Figure 4. DAC7654EVM Hardware Configuration

Table 4. Non-Default Setting of Jumpers for DAC7654EVM Board

DESIGNATOR	JUMPER POSITION		FUNCTION
	1-2	2-3	
W1	CLOSED	OPEN	DAC A Output Unipolar Mode
W6	CLOSED	–	Offset A Range Unipolar Mode
W7	CLOSED	–	Offset B Range Unipolar Mode
W8	CLOSED	–	Offset C Range Unipolar Mode

**Table 4. Non-Default Setting of Jumpers for DAC7654EVM Board (continued)**

DESIGNATOR	JUMPER POSITION		FUNCTION
	1-2	2-3	
W9	CLOSED	–	Offset D Range Unipolar Mode
W12	CLOSED	OPEN	DAC B Output Unipolar Mode
W13	CLOSED	OPEN	DAC C Output Unipolar Mode
W20	CLOSED	OPEN	DAC D Output Unipolar Mode
W25	CLOSED	OPEN	Single Supply Operation (V <sub>ss</sub> = AGND)



NOTE: This diagram is for illustration purposes only. See the EVM schematic for recommended topology.

**Figure 5. DAC7654 and MSP430F449 Hardware I/O**

### 3 ADC and DAC Operation

For information and an example of the TLC4541 Reset, Sampling, and Conversion process, see the application report [SLAA234](#). The discussion and software in that application report are applicable to this document.

For information and an example of the DAC7654 SPI serial interface timing, see application report [SLAA213](#). The discussion and software in that application report are applicable to this document.

#### 3.1 Analog Input Configuration

The magnitude of the input voltage signal that can be input to the ADC is 0 V to 5 V.

### 3.2 DAC Output Configuration

Because DAC channel A is connected to an external amplifier with a gain of two, as shown in [Figure 6](#), this channel has an amplitude range of 0 V to 5 V.

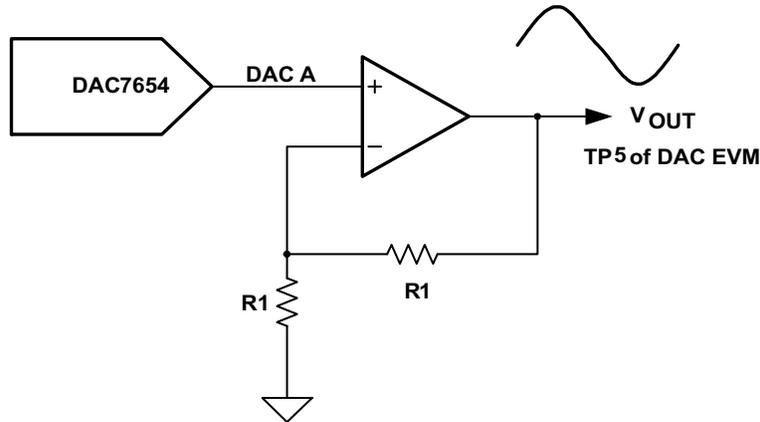


Figure 6. DAC A Output With a Gain of 2 (1 of 4 DACs)

If all the serial interface timing for both the TLC4541 ADC and the DAC7654 DAC are met, then it is possible to input an analog signal into the TLC4541EVM and to reproduce the signal from the DAC7654EVM.

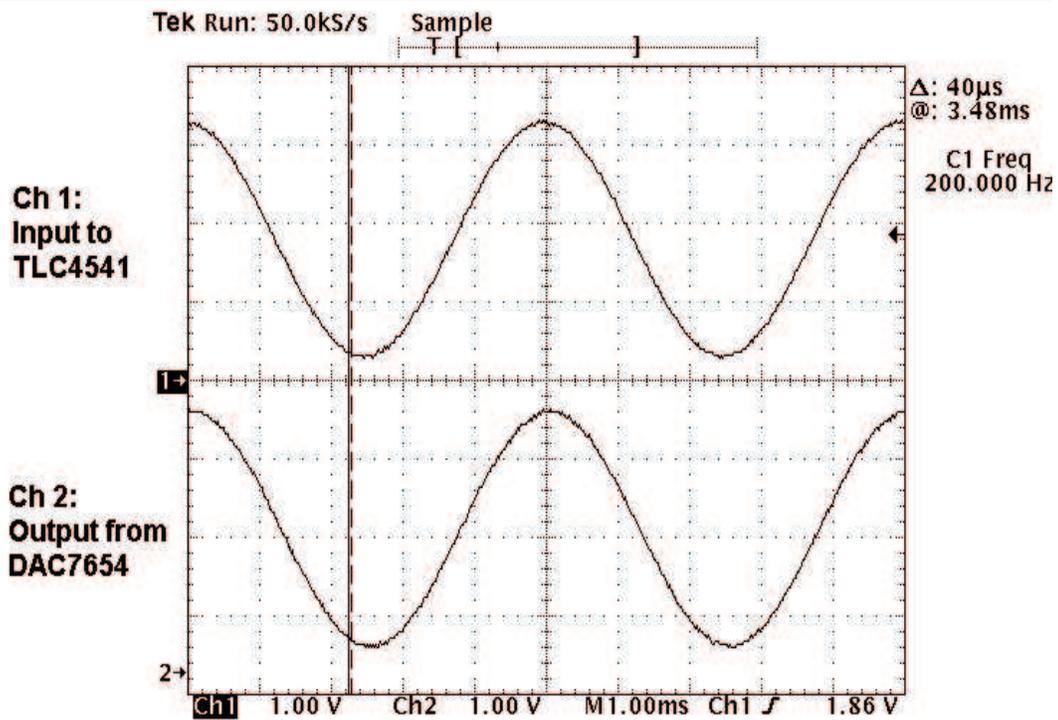


Figure 7. Input and Output Waveforms

[Figure 7](#) shows an oscilloscope trace of an input signal being applied to the ADC (channel 1) together with the resulting output signal from the DAC.

## 4 Software Development

The software for this application report was developed using TI's integrated development environment (IDE) for the MSP430 (IAR embedded workbench, Kickstart version).

### 4.1 Software Overview

Figure 8 shows an overview of the process, which is briefly described as follows.

- MSP430F449 setup occurs—including any GPIO pins that must perform special functions, and UART0 and UART1 are assigned as the SPI ports (UART0 for the TLC4541 and UART1 for the DAC5674).
- Following setup, the ADC is reset.
- The software continuously takes one sample from AIN0, storing the digital number in the hi\_byte and lo-byte variables.
- After the ADC takes the sample and digitizes it, the DAC then uses the digital value in the variables hi\_byte and lo-byte to generate an analog sample back out.
- The HPA449 board does not include an 8-MHz resonator, but the user can install one, if desired. The software allows the application to run without the resonator by simply defining the resonator as zero in the #define choice. A one should be selected if the resonator is installed.

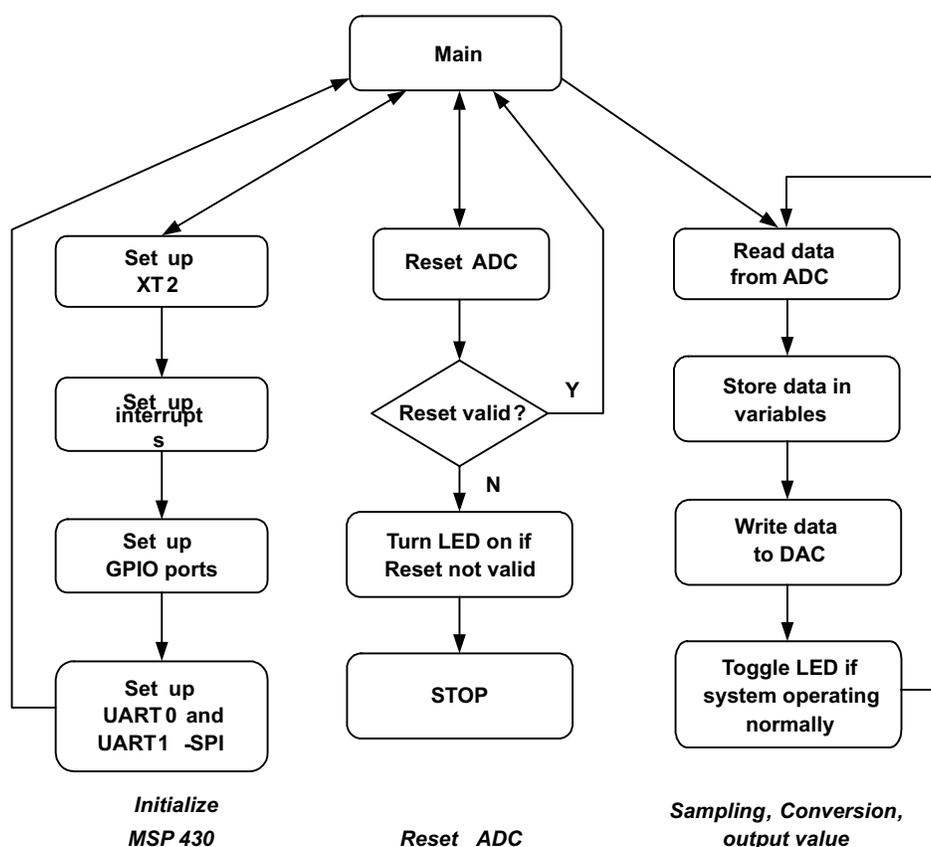


Figure 8. Software Overview

## 5 References

1. TLC4541, TLC4545, 5-V, Low Power, 16-Bit, 200-KSPS, Serial Analog-to-Digital Converters with Auto-Power Down data sheet ([SLAS293](#))
2. DAC7654, 16-Bit, Quad Voltage Output, Digital-to-Analog Converter data sheet ([SBAS263](#))
3. TLC4541EVM User's Guide ([SLAU103](#))
4. DAC7654 Evaluation Module User's Guide ([SLAU130](#))

5. MSP430x43x, MSP430x44x, Mixed Signal Microcontroller data sheet ([SLAS344](#))
6. MSP430F44x Evaluation System (HPA449) User's Guide (SoftBaugh, Inc.)
7. MSP430F4xx Family User's Guide ([SLU056](#))
8. Interfacing Low Power Serial (SPI) ADCs to the MSP430F449 ([SLAA234](#))
9. Interfacing the DAC7654 to the MSP430F449 ([SLAA213](#))

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