WP3211 Home Gateway Processor Data Sheet

1. Features

- WP3211 SOC integrated with a high performance 32-bit RISC processor. The processor contains 8K Instruction cache, 2K Data cache. Operation frequency is user selectable 125/100/75MHz. The processor supports Big/Little Endian Mode and EJTAG debug port.
- Supports 16M/64M/128M bit SDRAM with 2/4-bank size availability, its bus operation frequency matches processor core frequency.
- Two banks of Static Memory interfaces which can support Mask ROM, Page Mode ROM, EPROM, E2PROM, SRAM and NOR Flash (linear type)
- NAND Flash (block type) controller interfaces
- Provide a 256-Byte hard-wired boot code that can choose booting from normal ROM, NAND Flash, UART or EJTAG debugger interface
- PCMCIA-like interface to support glue-less connected to WLAN 802.11b device
- Internal two 10/100 Ethernet MAC
- 5 port 10/100 Ethernet switch and PHYs with Auto-MDIX integrated
- There are 4 bus masters on the WP3211 including CPU, Ethernet 1, Ethernet 2 and Memory-to-Memory DMA
- Three 24-bit up-count Timers and supports Interval timer mode and Watchdog timer modes (only Timer 3)
- Two sets of full duplex UARTs, one high speed up to 921K bps and one speed up to 115.2K bps
- Provide 16 bi-directional general-purpose I/O pins (shared with other function pins)
- 208 pins QFP Package

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2. System Diagram

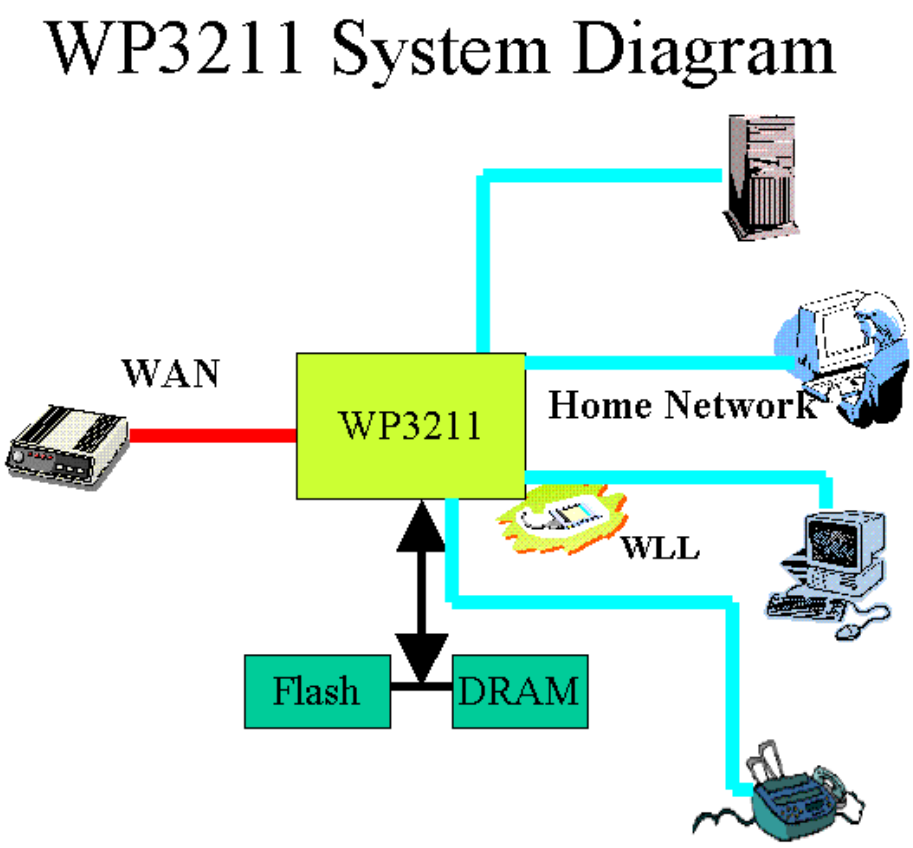

Figure 2-1 System Diagram

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3. Functional Description:

3.1. General Description

The WP3211 is a SOC for Home Gateway processor integrate a 32-bit RISC microprocessor core with a number of on-chip peripherals, including Interrupt Controller, Timer, Clock Generation Controller, Memory Interface, 5-port switch and PHY, Memory-to-Memory DMA and PCMCIA like interface …etc.

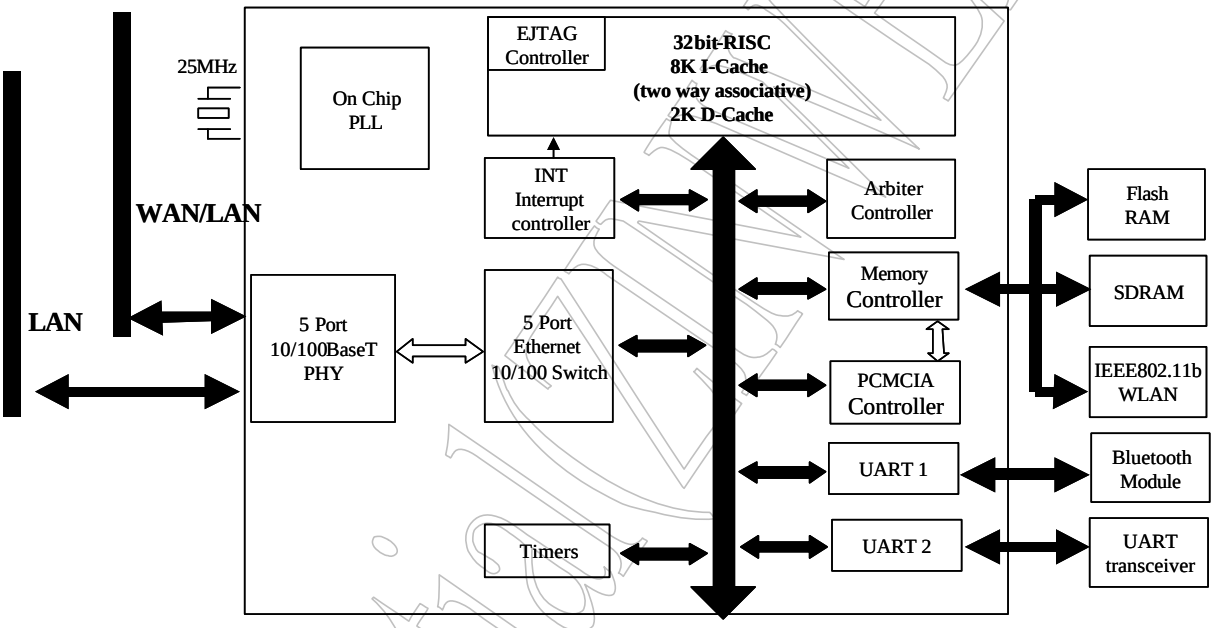

Figure 3-1 Functional Block Diagram

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3.2. Functional Description

3.2.1. CPU

- WP3211 integrated a high performance 32-bit RISC processor
- 8K bytes of Instruction cache (two-way associated)
- 2K bytes of Data cache (direct map)
- Support Big/Little Endian
- Support EJTAG debug interface
- Selectable 75MHz/100MHz/125MHz CPU clock

3.2.2. SDRAM Controller

- Supports 16M/64M/128M bit SDRAM with 2/4-bank size availability
- Support of 16/32-bit static bus size
- SDRAM clock speed is the same as CPU clock

3.2.3. Static Memory Controller

- Support Mask ROM, Page Mode ROM, EPROM, E2PROM, SRAM and NOR Flash (linear type)
- 2 banks of Static Memory interfaces
- 8-bit/16-bit static bus size independently per bank
- Supports memory sizes to 64M Byte per bank in 8-bit or16-bit mode

3.2.4. NAND Flash Controller

- Support NAND Flash (block type) controller interfaces

3.2.5. Boot code

- Provide a 256-Byte hard-wired boot code that can choose booting from normal ROM, NAND Flash, UART or EJTAG debugger interface

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3.2.6. Wireless LAN Interface

- PCMCIA-like interface to support glue-less connected to WLAN 802.11b device

3.2.7. Timer/Counter

- 3 24-bit up counter Timers
- Supports Interval timer mode and Watchdog timer modes (only Timer 3)
- Support of external input clock

3.2.8. Interrupt Controller

- Maskable Interrupts: up to 16 external interrupt inputs
- Each external interrupt can be edge or level sensitive

Interrupt Requested Via	Interrupt Vector	Default Priority
Timer	0x01	0 (highest)
DMAC	0x02	1
UART1	0x03	2
ETH1	0x04	3
ETH2	0x05	4
PCMCIA	0x06	5
Serial IO Bus	0x07	6
UART2	0x08	7
GPIO	0x09	8
Reserved	0xA	9
Arbiter	0x0B	A

Table 3-1 Tables of Interrupt Vector and Priority

3.2.9. Bus Maters and Direct Memory Access Controller (DMAC)

- There are 4 bus masters on the WP3211 including CPU, Ethernet 1, Ethernet 2 and Memory-to-Memory DMA
- Except CPU, each bus master has dedicated DMA controller with Tx/Rx.
- Support flexible descriptor based operation and chaining
- For each descriptor can transfer block size up to 20 bits
- The Memory-to-Memory DMA can support Memory mapped I/O to Memory, Memory-to-Memory mapped I/O and Memory to Memory transfer
- Supports of word aligned transfers using 1,4,8,16,32 words burst reads and writes to/from Memory

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3.2.10. UARTs

- 2 sets of full duplex UARTs, one high speed and one low speed
- High Speed UART support up to 921600 baud
- Low Speed UART support up to 115200 baud
- On-Chip Baud rate generator
- Modem flow control support
- High Speed UART supports 8-bit x 16 TX FIFO and 12-bit (8-bit data and 4-bit status) x 16 RX FIFO
- Low Speed UART supports 8-bit x 4 TX FIFO and 12-bit x 4 RX FIFO

3.2.11. Internal two 10/100 Ethernet MAC

- Two sets of 10/100, half or full duplex Ethernet Media Access Controller
- IEEE 802.3 full duplex flow control
- IP multicast receives and filter support using 64-bit hash table
- Receive early interrupt
- Transmit polling
- Auto pad insertion for short packets

3.2.12. 5-port Ethernet switch and transceivers

- Build in SSRAM for frame buffer
- Build in storage of 1K MAC address
- Support flow control
- Port base VLAN
- Integrate 5 ports Automatic MDI/MDI-X configuration transceiver
- Built in regulator for internal core usage

3.2.13. General Purpose I/O Interface

- Provide 16 bi-directional general-purpose I/O pins (shared with other function pins)
- Each general-purpose I/O pin can be independently configured as input, output, and bi-direction with interrupt function

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3.2.14. Clock Module

- Use one external 25MHz crystal or oscillator

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4. Memory Map

With the MMU, processor can access all the 32-bit address. How the virtual address is mapped to physical address is shown below:

Virtual Address Space	Description	Mapped to Physical Address
0xC000_0000 to 0xFFFF_FFFF	KSEG2. 1Gbyte. Addressable only in kernel mode. Cached.	0x0000_0000 to 0x1FFF_FFFF
0xA000_0000 to 0xBFFF_FFFF	KSEG1. 0.5Gbyte. Addressable only in kernel mode. Uncached. Used for I/O devices.	0x0000_0000 to 0x1FFF_FFFF
0x8000_0000 to 0x9FFF_FFFF	KSEG0. 0.5Gbyte. Addressable only in kernel mode. Cached.	0x0000_0000 to 0x1FFF_FFFF
0x0000_0000 to 0x7FFF_FFFF	KUSEG. 2Gbyte. Addressable in kernel or user mode. Cached.	0x0000_0000 to 0x1FFF_FFFF

Table 3-2 Table of Virtual Address Mapping

How the physical address mapping is shown in following table:

Physical Address Range	Devices
0x1C00-0000 - 0x1FFF-FFFF (64MB)	ROM bank1, memory mapped I/O
0x1800-0000 - 0x1BFF-FFFF (64MB)	ROM bank2, Memory mapped I/O
0x1400-0000 - 0x17FF-FFFF (64MB)	System control registers
0x1300-0000 - 0x13FF-FFFF (16MB)	WLAN Socket Common space
0x1200-0000 - 0x12FF-FFFF (16MB)	WLAN Socket Attribute space
0x1100-0000 - 0x11FF-FFFF (16MB)	Reserved
0x1000-0000 - 0x10FF-FFFF (16MB)	WLAN Socket I/O space
0x0800-0000 - 0x0FFF-FFFF (128MB)	Reserved
0x0000-0000 - 0x07FF-FFFF (128MB)	SDRAM bank

Table 3-3 Physical Address Mapping

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5. Pin Descriptions

The tables of pin show the Internal Pull Up or Internal Down and their level.

5.1. System Reset Pins

Group	Name	I/O	Description	Pin No.	Level	Pull
Reset	GRESET_I	I	System Reset Input	36	CMOS	UP

5.2. Crystal Pins

Group	Name	I/O	Description	Pin No.	Level	Pull
XIN	X2	O	Crystal Pad Output	152	Analog	
	OSCI	I	Crystal Pad Input	153	Analog	

5.3. Common Memory Interface

Group	Name	I/O	Description	Pin No.	Level	Pull
Data	MDATA_0_B	IO	Memory Data Bus bit 0	92	CMOS	
	MDATA_1_B	IO	Memory Data Bus bit 1	93	CMOS	
	MDATA_2_B	IO	Memory Data Bus bit 2	94	CMOS	
	MDATA_3_B	IO	Memory Data Bus bit 3	95	CMOS	
	MDATA_4_B	IO	Memory Data Bus bit 4	96	CMOS	
	MDATA_5_B	IO	Memory Data Bus bit 5	97	CMOS	
	MDATA_6_B	IO	Memory Data Bus bit 6	98	CMOS	
	MDATA_7_B	IO	Memory Data Bus bit 7	99	CMOS	
	MDATA_8_B	IO	Memory Data Bus bit 8	100	CMOS	
	MDATA_9_B	IO	Memory Data Bus bit 9	101	CMOS	
	MDATA_10_B	IO	Memory Data Bus bit 10	102	CMOS	
	MDATA_11_B	IO	Memory Data Bus bit 11	105	CMOS	
	MDATA_12_B	IO	Memory Data Bus bit 12	106	CMOS	
	MDATA_13_B	IO	Memory Data Bus bit 13	107	CMOS	
	MDATA_14_B	IO	Memory Data Bus bit 14	108	CMOS	
	MDATA_15_B	IO	Memory Data Bus bit 15	109	CMOS	
	MDATA_16_B	IO	Memory Data Bus bit 16/Memory Address Bus bit 13	110	CMOS	
	MDATA_17_B	IO	Memory Data Bus bit 17/Memory Address Bus bit 14	111	CMOS	
	MDATA_18_B	IO	Memory Data Bus bit 18/Memory Address Bus bit 15	112	CMOS	
	MDATA_19_B	IO	Memory Data Bus bit 19/Memory Address Bus bit 16	113	CMOS	
	MDATA_20_B	IO	Memory Data Bus bit 20/Memory Address Bus bit 17	116	CMOS	
	MDATA_21_B	IO	Memory Data Bus bit 21/Memory Address Bus bit 18	117	CMOS	
	MDATA_22_B	IO	Memory Data Bus bit 22/Memory Address Bus bit 19	118	CMOS	
	MDATA_23_B	IO	Memory Data Bus bit 23/Memory Address Bus bit 20	119	CMOS	
	MDATA_24_B	IO	Memory Data Bus bit 24/Memory Address Bus bit 21	120	CMOS	
	MDATA_25_B	IO	Memory Data Bus bit 25/Memory Address Bus bit 22	121	CMOS	

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Group	Name	I/O	Description	Pin No.	Level	Pull
	MDATA_26_B	IO	Memory Data Bus bit 26/Memory Address Bus bit 23	124	CMOS	
	MDATA_27_B	IO	Memory Data Bus bit 27/Memory Address Bus bit 24	125	CMOS	
	MDATA_28_B	IO	Memory Data Bus bit 28/Memory Address Bus bit 25	126	CMOS	
	MDATA_29_B	IO	Memory Data Bus bit 29	127	CMOS	
	MDATA_30_B	IO	Memory Data Bus bit 30	128	CMOS	
	MDATA_31_B	IO	Memory Data Bus bit 31	129	CMOS	
Address/ Power On Configuration	MADDR_0_B	IO	Memory Address Bus bit 0	75	CMOS	
	MADDR_1_B	IO	Memory Address Bus bit 1	74	CMOS	
	MADDR_2_B	IO	Memory Address Bus bit 2	73	CMOS	
	MADDR_3_B	IO	Memory Address Bus bit 3	72	CMOS	
	MADDR_4_B	IO	Memory Address Bus bit 4	71	CMOS	
	MADDR_5_B	IO	Memory Address Bus bit 5	70	CMOS	
	MADDR_6_B	IO	Memory Address Bus bit 6	67	CMOS	
	MADDR_7_B	IO	Memory Address Bus bit 7	66	CMOS	
	MADDR_8_O	O	Memory Address Bus bit 8	65	CMOS	
Address	MADDR_9_O	O	Memory Address Bus bit 9	64	CMOS	
	MADDR_10_O	O	Memory Address Bus bit 10	63	CMOS	
	MADDR_11_O	O	Memory Address Bus bit 11	62	CMOS	
	MADDR_12_O	O	Memory Address Bus bit 12	61	CMOS	
	MI_WE_O	O	Memory Bus Write Enable	85	CMOS	

5.4. Static Memory Interface

Group	Name	I/O	Description	Pin No.	Level	Pull
ROM	CE_ROM_1_O	O	Chips Select Enable of ROM Bank 1	49	CMOS	
	CE_ROM_2_O	O	Chips Select Enable of ROM Bank 2	50	CMOS	

5.5. SDRAM Interface

Group	Name	I/O	Description	Pin No.	Level	Pull
	CLK_SDRAM_O	O	SDRAM Clock	87	CMOS	
	DQM_SDRAM_0_O	O	SDRAM Data Byte 0 (bit 7:0) Enable/ROM Bank 1 Output Enable	90	CMOS	
	DQM_SDRAM_1_O	O	SDRAM Data Byte 1 (bit 15:8) Enable/ROM Bank 2 Output Enable	89	CMOS	
	DQM_SDRAM_2_O	O	SDRAM Data Byte 2 (bit 23:16) Enable/PCMCIA Memory Space Output Enable	77	CMOS	
	DQM_SDRAM_3_O	O	SDRAM Data Byte 3 (bit 31:24) Enable/ PCMCIA Memory Space Write Enable	76	CMOS	
	MI_CAS_O	O	SDRAM Column Address Strobe/ROM Lower Byte Output Enable	84	CMOS	
	MI_RAS_O	O	SDRAM Row Address Strobe/ ROM Higher Byte Output Enable	83	CMOS	
	CE_SDRAM_O	O	Chip Enable of SDRAM Bank	80	CMOS	
	BA0_SDRAM_O	O	SDRAM Bank Address 0	79	CMOS	
SDRAM	BA1_SDRAM_O	O	SDRAM Bank Address 1/PCMCIA Attribute Space Selection	78	CMOS	

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5.6. NAND Flash Interface

Group	Name	I/O	Description	Pin No.	Level	Pull
NAND	WE_FLASH_O	O	NAND FLASH Write Enable	28	CMOS	
	ALE_FLASH_O	O	NAND Flash Address Latch Enable	27	CMOS	
	CLE_FLASH_O	O	NAND Flash Command Latch Enable	26	CMOS	
	RE_FLASH_O	O	NAND FLASH READ Enable	29	CMOS	
	CE_FLASH_O	O	NAND Flash Chip Selection Enable	30	CMOS	
	RB_ROM_I	I	NAND Flash Ready/Busy/PCMCIA PWAIT	55	CMOS	UP

5.7. PCMCIA Interface

Group	Name	I/O	Description	Pin No.	Level	Pull
PCMCIA	CE_PCMC_1_O	O	PCMCIA Card Select, Low Byte	56	CMOS	
	CE_PCMC_2_O	O	PCMCIA Card Select, High Byte	57	CMOS	

5.8. UART and GPIO Interface

Group	Name	I/O	Description	Pin No.	Level	Pull
UART1/ GPIO	UART1_TXD_O	O	UART1 Transmit Data	130	CMOS	
	UART1_RXD_I	I	UART1 Receive Data	133	CMOS	Up
	UART1_CTS_I	I/O	UART1 Clear to Send/GPIO_S_1_B	132	CMOS	
	UART1_RTS_O	I/O	UART1 Request To Send/GPIO_S_2_B	131	CMOS	
UART2/GPIO	UART2_TXD_O	I/O	UART2 Transmit Data/GPIO_S_5_B	16	CMOS	
	UART2_RXD_I	I/O	UART2 Receive Data/ GPIO_S_9_B	19	CMOS	
	UART2_CTS_I	I/O	UART2 Clear to Send/ GPIO_S_11_B	18	CMOS	
	UART2_RTS_O	I/O	UART2 Request To Send / GPIO_S_10_B	17	CMOS	
	UART2_DSR_I	I/O	UART2 Data Set Ready / GPIO_S_3	21	CMOS	
	UART2_DTR_O	I/O	UART2 Data Transmit Ready / GPIO_S_4	20	CMOS	
	UART2_RI_I	I	UART2 Ring Indicator/ EJTAG Clock Input	37	CMOS	Up
	UART2_DCD_I	I	UART2 Data Carrier Detect/ EJTAG Data Input	40	CMOS	Up
GPIO	GPIO_S_6_B	I/O	GPIO 6	24	CMOS	
	GPIO_S_7_B	I/O	GPIO 7 / External Clock source of Timer module	25	CMOS	
	GPIO_S_8_B	I/O	GPIO 8	48	CMOS	
	GPIO_S_12_B	I/O	GPIO 12 / PCMCIA Card Reset	58	CMOS	
	GPIO_S_13_B	I/O	GPIO 13 / PCMCIA RDY/IREQ	59	CMOS	
	GPIO_S_14_B	I/O	GPIO 14 / PCMCIA STSCHG	60	CMOS	
	GPIO_S_15_B	I/O	GPIO 15	15	CMOS	
	GPIO_S_16_B	I/O	GPIO 16	14	CMOS	

5.9. Two-wire serial Interface

Group	Name	I/O	Description	Pin No.	Level	Pull
EEPROM	SCL	O	Two-wire serial clock output	10	CMOS	
	SDA	I/O	Two-wire serial data	11	CMOS	

5.10. Switch Interface

Group	Name	I/O	Description	Pin No.	Level	Pull
RXI	RXIP0	I	Twist Pair Port 0 positive input	156	Analog	
	RXIM0	I	Twist Pair Port 0 negative input	161	Analog	

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Group	Name	I/O	Description	Pin No.	Level	Pull
	RXIP1	I	Twist Pair Port 1 positive input	172	Analog	
	RXIM1	I	Twist Pair Port 1 negative input	173	Analog	
	RXIP2	I	Twist Pair Port 2 positive input	183	Analog	
	RXIM2	I	Twist Pair Port 2 negative input	184	Analog	
	RXIP3	I	Twist Pair Port 3 positive input	195	Analog	
	RXIM3	I	Twist Pair Port 3 negative input	196	Analog	
	RXIP4	I	Twist Pair Port 4 positive input	199	Analog	
	RXIM4	I	Twist Pair Port 4 negative input	200	Analog	
TXO	TXOP0	O	Twist Pair Port 0 positive Output	163	Analog	
	TXOM0	O	Twist Pair Port 0 negative Output	164	Analog	
	TXOP1	O	Twist Pair Port 1 positive Output	169	Analog	
	TXOM1	O	Twist Pair Port 1 negative Output	170	Analog	
	TXOP2	O	Twist Pair Port 2 positive Output	186	Analog	
	TXOM2	O	Twist Pair Port 2 negative Output	187	Analog	
	TXOP3	O	Twist Pair Port 3 positive Output	192	Analog	
	TXOM3	O	Twist Pair Port 3 negative Output	193	Analog	
	TXOP4	O	Twist Pair Port 4 positive Output	202	Analog	
	TXOM4	O	Twist Pair Port 4 negative Output	1	Analog	
Band Gap	BGRES	I/O	Band gap resister. It is connected to GND through a 6.2k-ohm resistor in application circuit.	176	Analog	
REG	REG_OUT	O	Regulator output It is used to control external transistor to generate a stable 2.5v voltage source.	150	Analog	
LED SPEED	LED_SPEED_0_B	O	Speed (output after reset)	42	CMOS	
	LED_SPEED_1_B	O	Speed (output after reset)	45	CMOS	
	LED_SPEED_2_B	O	Speed (output after reset)	136	CMOS	
	LED_SPEED_3_B	O	Speed (output after reset)	139	CMOS	
	LED_SPEED_4_B	O	Speed (output after reset)	142	CMOS	
LED FULL	LED_FULL_0_B	O	Full/half, Link (output after reset)	43	CMOS	
	LED_FULL_1_B	O	Full/half, Link (output after reset)	46	CMOS	
	LED_FULL_2_B	O	Full/half, Link (output after reset)	137	CMOS	
	LED_FULL_3_B	O	Full/half, Link (output after reset)	140	CMOS	
	LED_FULL_4_B	O	Full/half, Link (output after reset)	143	CMOS	
LED LINK	LED_LINK_0_B	O	Link, Activity (output after reset)	41	CMOS	
	LED_LINK_1_B	O	Link, Activity (output after reset)	44	CMOS	
	LED_LINK_2_B	O	Link, Activity (output after reset)	47	CMOS	
	LED_LINK_3_B	O	Link, Activity (output after reset)	138	CMOS	
	LED_LINK_4_B	O	Link, Activity (output after reset)	141	CMOS	

Test Interface

Group	Name	I/O	Description	Pin No.	Level	Pull
	Test1	I	Switch Test mode selection It should be connected to GND for normal operation 1: test mode, 0: normal	31	CMOS	Down

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Group	Name	I/O	Description	Pin No.	Level	Pull
	Test2	I	Switch Test mode selection It should be connected to GND for normal operation 1: Switch operation, 0: Network Processor operation (default) When Test1 is '1', Test2 determine which module will connect to input or output port.	32	CMOS	Down
Test	JTAG_TMS_I	I	EJTAG Test Mode Select	38	CMOS	Down
	TESTM_I	I	SCAN Test Mode	35	CMOS	Down
	SCANEN_I	I	SCAN Test Mode Test Data select	34	CMOS	Down
	TEST_UNPLL_I	I	Bypass PLLs	33	CMOS	Down
	RMBIST_O	O	RAM BIST Output/ EJTAG Test Data Output	39	CMOS	

5.11. Power/Ground

Group	Name	Description	Level	Pin Numbers
Power/ Ground	DVCC	Digital Power	2.5 V	5,6,9,13,54,81,114,144,145,146,154
	AVCC	Analog Power	2.5 V	3, 162,166,167,171,175,185,189,190,194,201
	GND	Ground	Ground	2,4,7,8,12,23,52,53,69,82,88,91,104,115,123,147,148,149,151,155,165,168,174,177,182,188,191,197,198
	VDDIO	External I/O Power	3.3 V	22,51,68,86,103,122,
	VDDPLL	PLL Power	2.5 V	134
	VSSPLL	PLL Ground	Ground	135
NC	NC	No Connected		157,158,159,160,161,163,164,178,179,180,181,203,204,205,206,207,208

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6. Electrical Characteristics

6.1. Absolute Maximum Rating

Symbol	Parameter	Value	Unit
Tstg	Storage temperature	-65 ~ 150	℃
Vcc	Input Voltage	6	V
Tj	Junction Temperature	Max 125	℃
ESD	ESD Protection	2000	V

6.2. Recommended Operation Condition

Symbol	Parameter	Min	Typ	Max	Unit
Vopt	Operation Temperature	-40		70	℃
Vcc_io	I/O Supply Voltage	3.0	3.3	3.6	V
Vcc	Core Supply Voltage	2.25	2.5	2.75	V
V_{IH}	Logical Input High	1.8	3.3	3.6	V
V_{IL}	Logical Input Low	-0.5		1.0	V
V_{OH}	Logical Output High	2.4			V
V_{OL}	Logical Output Low			0.4	V

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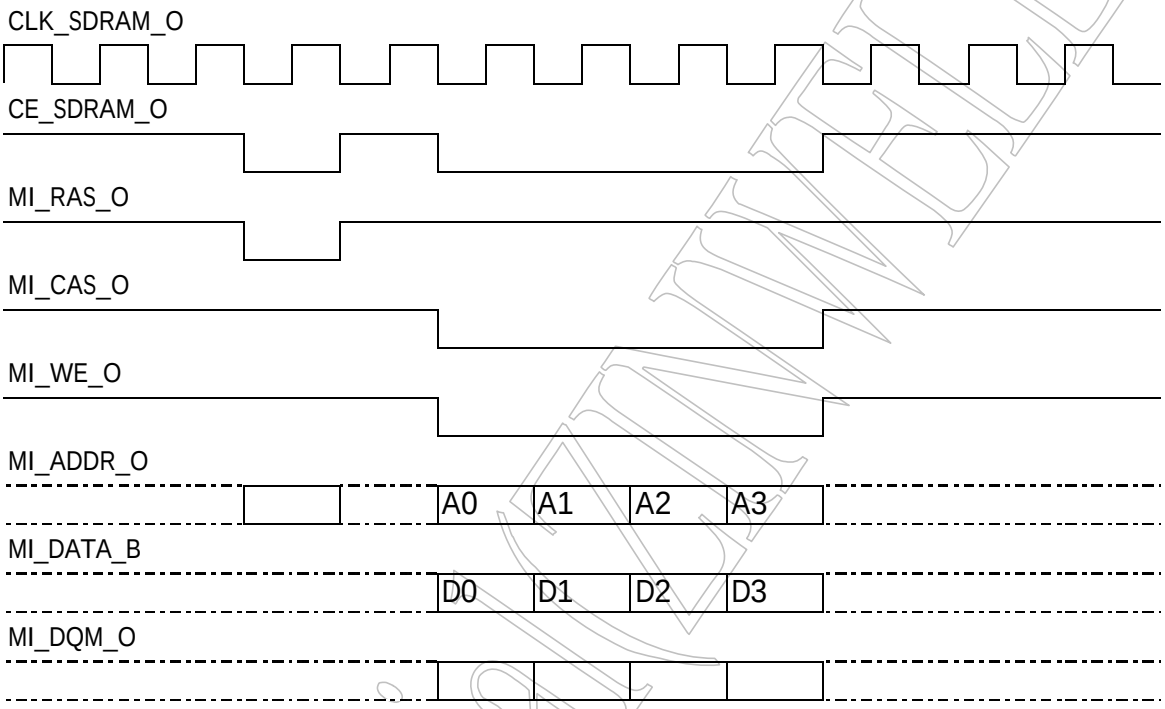
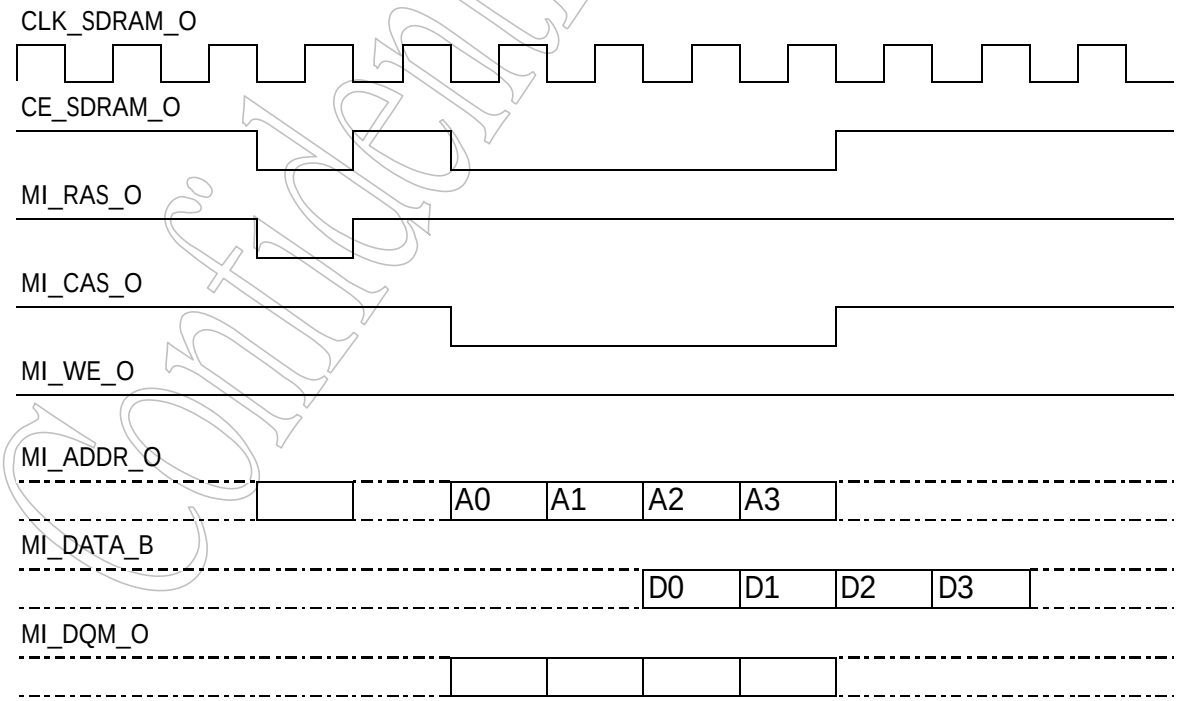
7. AC Specification

7.1. SDRAM Interface

SDRAM Write Timing (CAS = 2)



SDRAM Read Timing (CAS = 2)



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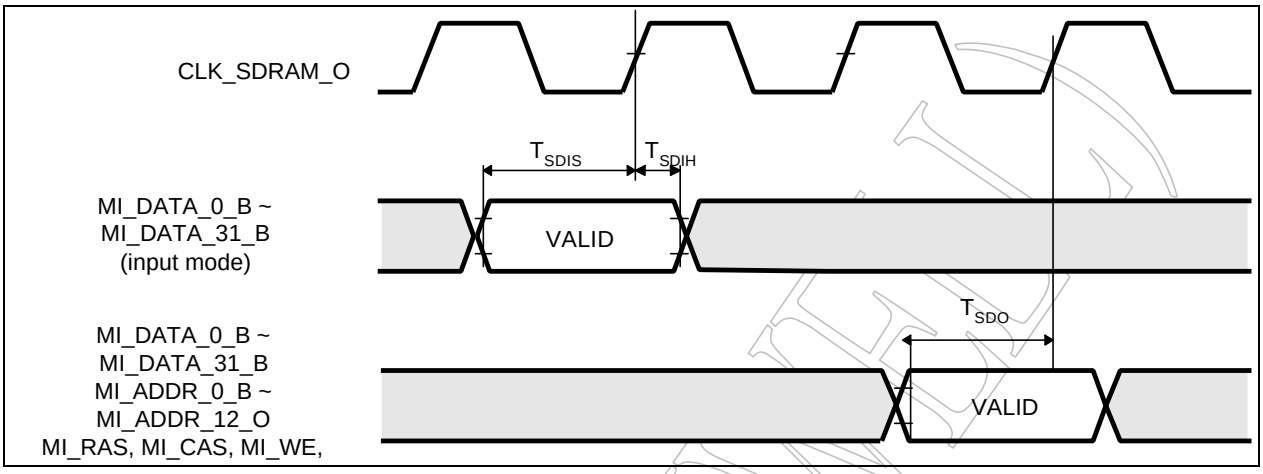
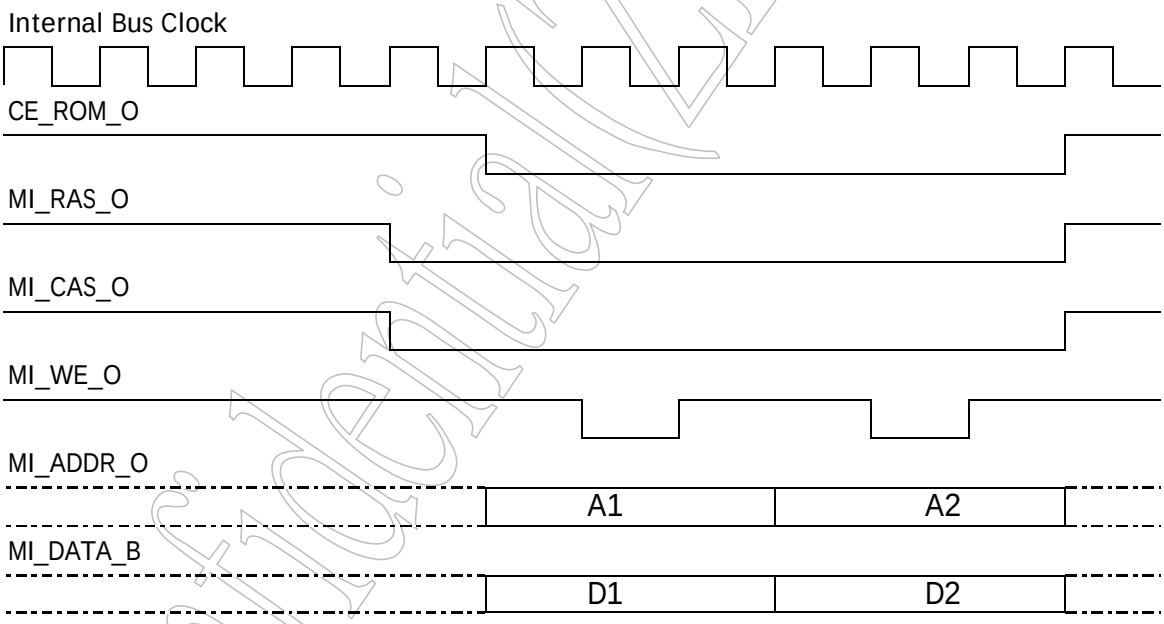


7.2. SRAM/FLASH Interface

SRAM/FLASH Write Timing (For 16-bit interface, ROMCR = 0x0)



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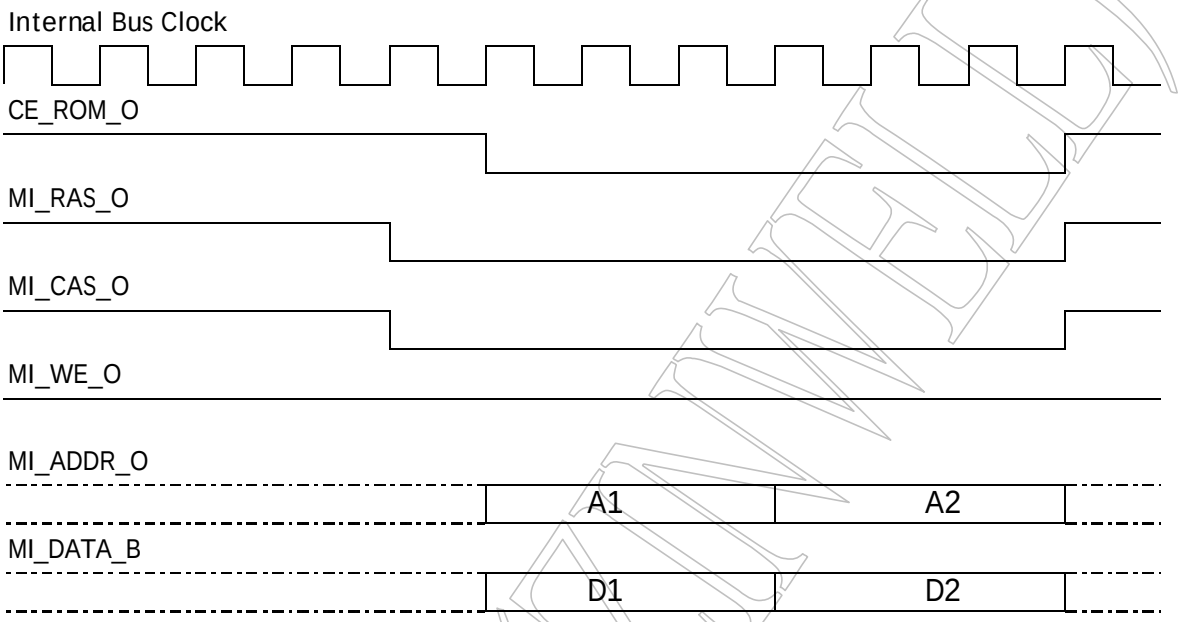
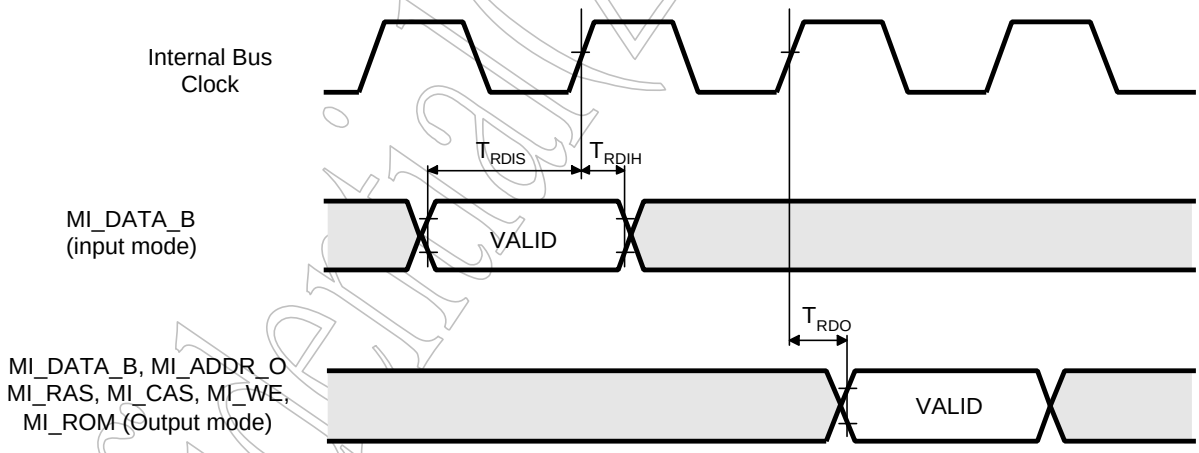
SRAM/FLASH Read Timing (For 16-bit interface, ROMCR = 0x0)





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7.3. AC OPERATING TEST CONDITIONS (VDD = 3.3V ±0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0	V
Input timing measurement reference level	1.4	V
Input rise and fall time	Tr/Tf = 1/1	Ns
Output timing measurement reference level	1.4	V
Output load condition	25	pF

7.4. OPERATING AC PARAMETER

Parameter	Min. Value	Max. value	Unit
T_{SDIS}	3	-	Ns
T_{SDIH}	1	-	Ns
T_{SDO}	3	-	Ns
T_{RDIS}	6	-	Ns
T_{RDIH}	3	-	Ns
T_{RDO}	-	12	Ns

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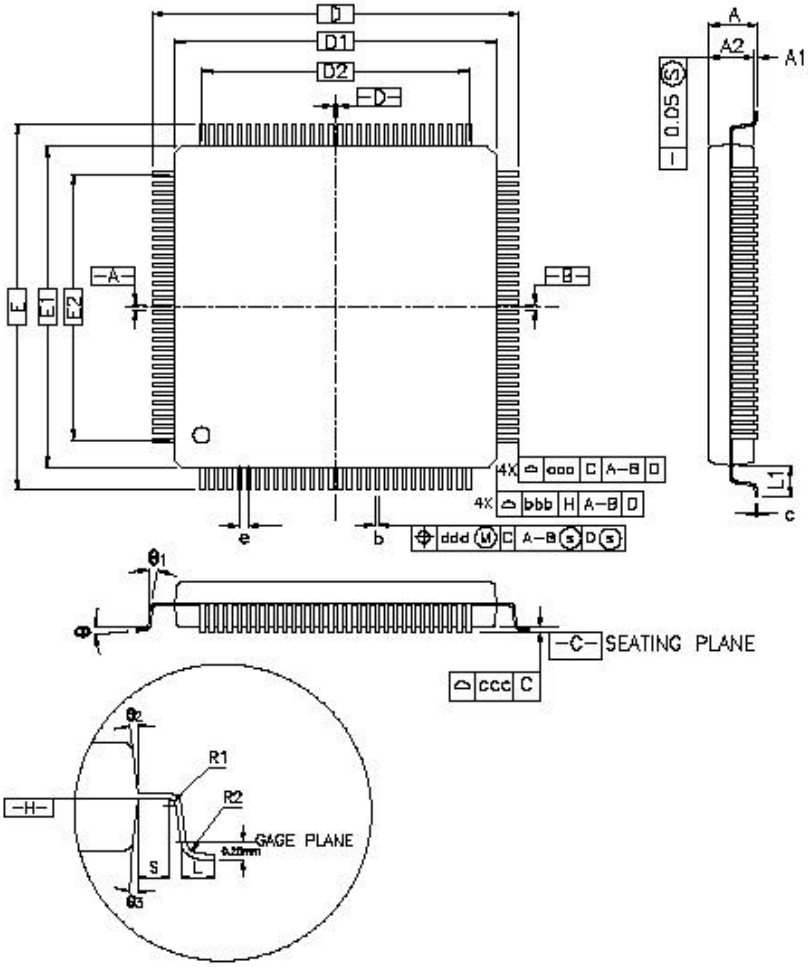
8. Packaging

The Home Gateway processor WP3211 is available in a 208-pin QFP package (28x28mm). Figure 8-1 shows the mechanical drawing for the 208-pin QFP package.



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A1	0.25	—	—	0.010	—	—
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	30.60 BSC.			1.205 BSC.		
D1	28.00 BSC.			1.102 BSC.		
E	30.60 BSC.			1.205 BSC.		
E1	28.00 BSC.			1.102 BSC.		
R2	0.08	—	0.25	0.003	—	0.010
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	8° REF			8° REF		
θ3	8° REF			8° REF		
c	0.09	0.15	0.20	0.004	0.006	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.30 REF			0.051 REF		
S	0.20	—	—	0.008	—	—

Figure 8-1 208-pin QFP Mechanical Drawing

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