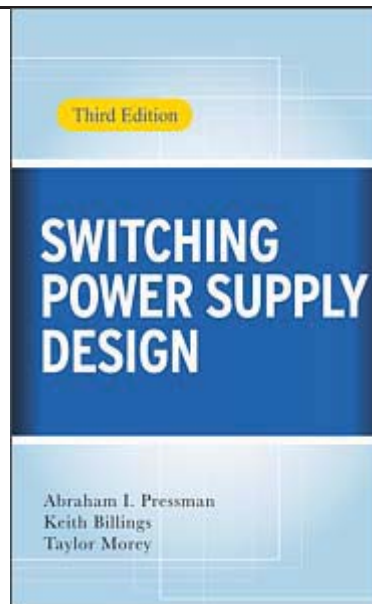


Third Edition

# SWITCHING POWER SUPPLY DESIGN

Abraham I. Pressman  
Keith Billings  
Taylor Morey



**FINAL**

# Switching Power Supply Design

Third Edition

*Abraham I. Pressman*

*Keith Billings*

*Taylor Morey*



New York Chicago San Francisco Lisbon London Madrid Mexico City Milan New Delhi  
San Juan Seoul Singapore Sydney Toronto

---

---

**The McGraw-Hill Companies**

---

**Library of Congress Cataloging-in-Publication Data**

McGraw-Hill books are available at special quantity discounts to use as premiums and sales promotions, or for use in corporate training programs. To contact a special sales representative, please visit the Contact Us page at [www.mhprofessional.com](http://www.mhprofessional.com).

**Switching Power Supply Design, Third Edition**

Copyright © 2009 by The McGraw-Hill Companies.

All rights reserved. Printed in the United States of America. Except as permitted under the Copyright Act of 1976, no part of this publication may be reproduced or distributed in any form or by any means, or stored in a database or retrieval system, without the prior written permission of publisher.

1234567890 DOC DOC 019

ISBN 978-0-07-148272-1

MHID 0-07-148272-5

**Sponsoring Editor**

Wendy Rinaldi

**Acquisitions Coordinator**

Joya Anthony

**Production Supervisor**

George Anderson

**Art Director, Cover**

Jeff Weeks

**Editorial Supervisor**

Janet Walden

**Proofreader**

Paul Tyler

**Composition**

International Typesetting and Composition

**Cover Designer**

Jeff Weeks

**Project Editor**

LeeAnn Pickrell

**Indexer**

Ted Laux

**Illustration**

International Typesetting and Composition

Information has been obtained by McGraw-Hill from sources believed to be reliable. However, because of the possibility of human or mechanical error by our sources, McGraw-Hill, or others, McGraw-Hill does not guarantee the accuracy, adequacy, or completeness of any information and is not responsible for any errors or omissions or the results obtained from the use of such information.

---

**In fond memory of Abraham Pressman, master of the art, 1915 – 2001.  
Immortalized by his timeless writings and his legacy—a gift  
of knowledge for future generations.**

**To Anne Pressman, for her help and encouragement  
on the third edition.**

**To my wife Diana for feeding the brute and allowing him  
to neglect her, yet again!**

---



## About the Authors

**Abraham I. Pressman** was a nationally known power supply consultant and lecturer. His background ranged from an Army radar officer to over four decades as an analog-digital design engineer in industry. He held key design roles in a number of significant “firsts” in electronics over more than a half century: the first particle accelerator to achieve an energy over one billion volts, the first high-speed printer in the computer industry, the first spacecraft to take pictures of the moon’s surface, and two of the earliest textbooks on computer logic circuit design using transistors and switching power supply design, respectively.

Mr. Pressman was the author of the first two editions of *Switching Power Supply Design*.

**Keith Billings** is a Chartered Electronic Engineer and author of the *Switchmode Power Supply Handbook*, published by McGraw-Hill. Keith spent his early years as an apprentice mechanical instrument maker (at a wage of four pounds a week) and followed this with a period of regular service in the Royal Air Force, servicing navigational instruments including automatic pilots and electronic compass equipment. Keith went into government service in the then Ministry of War and specialized in the design of special test equipment for military applications, including the UK3 satellite. During this period, he became qualified to degree standard by an arduous eight-year stint of evening classes (in those days, the only avenue open to the lower middle-class in England). For the last 44 years, Keith has specialized in switchmode power supply design and manufacturing. At the age of 75, he still remains active in the industry and owns the consulting company DKB Power, Inc., in Guelph, Canada. Keith presents the late Abe Pressman’s four-day course on power supply design (now converted to a Power Point presentation) and also a one-day course of his own on magnetics, which is the design of transformers and inductors. He is now a recognized expert in this field. It is a sobering thought to realize he now earns more in one day than he did in a whole year as an apprentice.

---

Keith was an avid yachtsman for many years, but he now flies gliders as a hobby, having built a high-performance sailplane in 1993. Keith “touched the face of god,” achieving an altitude of 22,000 feet in wave lift at Minden, Nevada, in 1994.

**Taylor Morey**, currently a professor of electronics at Conestoga College in Kitchener, Ontario, Canada, is coauthor of an electronics devices textbook and has taught courses at Wilfred Laurier University in Waterloo. He collaborates with Keith Billings as an independent power supply engineer and consultant and previously worked in switchmode power supply development at Varian Canada in Georgetown and Hammond Manufacturing and GFC Power in Guelph, where he first met Keith in 1988. During a five-year sojourn to Mexico, he became fluent in Spanish and taught electronics engineering courses at the Universidad Católica de La Paz and English as a second language at CIBNOR biological research institution of La Paz, where he also worked as an editor of graduate biology students’ articles for publication in refereed scientific journals. Earlier in his career, he worked for IBM Canada on mainframe computers and at Global TV’s studios in Toronto.

---



# Contents

Acknowledgments	xxxiii
Preface	xxxv

## Part I Topologies

<b>1 Basic Topologies</b>	<b>3</b>
1.1 Introduction to Linear Regulators and Switching Regulators of the Buck Boost and Inverting Types	3
1.2 Linear Regulator—the Dissipative Regulator	4
1.2.1 Basic Operation	4
1.2.2 Some Limitations of the Linear Regulator	6
1.2.3 Power Dissipation in the Series-Pass Transistor	6
1.2.4 Linear Regulator Efficiency vs. Output Voltage	7
1.2.5 Linear Regulators with PNP Series-Pass Transistors for Reduced Dissipation	9
1.3 Switching Regulator Topologies	10
1.3.1 The Buck Switching Regulator	10
1.3.1.1 Basic Elements and Waveforms of a Typical Buck Regulator	11
1.3.1.2 Buck Regulator Basic Operation	13
1.3.2 Typical Waveforms in the Buck Regulator	14
1.3.3 Buck Regulator Efficiency	15
1.3.3.1 Calculating Conduction Loss and Conduction-Related Efficiency	16
1.3.4 Buck Regulator Efficiency Including AC Switching Losses	16
1.3.5 Selecting the Optimum Switching Frequency	20
1.3.6 Design Examples	21
1.3.6.1 Buck Regulator Output Filter Inductor (Choke) Design	21
1.3.6.2 Designing the Inductor to Maintain Continuous Mode Operation	25
1.3.6.3 Inductor (Choke) Design	26

1.3.7 Output Capacitor	27
1.3.8 Obtaining Isolated Semi-Regulated Outputs from a Buck Regulator	30
1.4 The Boost Switching Regulator Topology	31
1.4.1 Basic Operation	31
1.4.2 The Discontinuous Mode Action in the Boost Regulator	33
1.4.3 The Continuous Mode Action in the Boost Regulator	35
1.4.4 Designing to Ensure Discontinuous Operation in the Boost Regulator	37
1.4.5 The Link Between the Boost Regulator and the Flyback Converter	40
1.5 The Polarity Inverting Boost Regulator	40
1.5.1 Basic Operation	40
1.5.2 Design Relations in the Polarity Inverting Boost Regulator	42
References	43
<b>2 Push-Pull and Forward Converter Topologies</b>	<b>45</b>
2.1 Introduction	45
2.2 The Push-Pull Topology	45
2.2.1 Basic Operation (With Master/Slave Outputs)	45
2.2.2 Slave Line-Load Regulation	48
2.2.3 Slave Output Voltage Tolerance	49
2.2.4 Master Output Inductor Minimum Current Limitations	49
2.2.5 Flux Imbalance in the Push-Pull Topology (Staircase Saturation Effects)	50
2.2.6 Indications of Flux Imbalance	52
2.2.7 Testing for Flux Imbalance	55
2.2.8 Coping with Flux Imbalance	56
2.2.8.1 Gapping the Core	56
2.2.8.2 Adding Primary Resistance	57
2.2.8.3 Matching Power Transistors	57
2.2.8.4 Using MOSFET Power Transistors	58
2.2.8.5 Using Current-Mode Topology	58
2.2.9 Power Transformer Design Relationships	59
2.2.9.1 Core Selection	59
2.2.9.2 Maximum Power Transistor On-Time Selection	60
2.2.9.3 Primary Turns Selection	61
2.2.9.4 Maximum Flux Change (Flux Density Swing) Selection	61
2.2.9.5 Secondary Turns Selection	63

---

---

2.2.10 Primary, Secondary Peak and rms Currents	63
2.2.10.1 Primary Peak Current Calculation	63
2.2.10.2 Primary rms Current Calculation and Wire Size Selection	64
2.2.10.3 Secondary Peak, rms Current, and Wire Size Calculation	65
2.2.10.4 Primary rms Current, and Wire Size Calculation	66
2.2.11 Transistor Voltage Stress and Leakage Inductance Spikes	67
2.2.12 Power Transistor Losses	69
2.2.12.1 AC Switching or Current-Voltage “Overlap” Losses	69
2.2.12.2 Transistor Conduction Losses	70
2.2.12.3 Typical Losses: 150-W, 50-kHz Push-Pull Converter	71
2.2.13 Output Power and Input Voltage Limitations in the Push-Pull Topology	71
2.2.14 Output Filter Design Relations	73
2.2.14.1 Output Inductor Design	73
2.2.14.2 Output Capacitor Design	74
2.3 Forward Converter Topology	75
2.3.1 Basic Operation	75
2.3.2 Design Relations: Output/Input Voltage, “On” Time, Turns Ratios	78
2.3.3 Slave Output Voltages	80
2.3.4 Secondary Load, Free-Wheeling Diode, and Inductor Currents	81
2.3.5 Relations Between Primary Current, Output Power, and Input Voltage	81
2.3.6 Maximum Off-Voltage Stress in Power Transistor	82
2.3.7 Practical Input Voltage/Output Power Limits	83
2.3.8 Forward Converter With Unequal Power and Reset Winding Turns	84
2.3.9 Forward Converter Magnetics	86
2.3.9.1 First-Quadrant Operation Only	86
2.3.9.2 Core Gapping in a Forward Converter	88
2.3.9.3 Magnetizing Inductance with Gapped Core	89
2.3.10 Power Transformer Design Relations	90
2.3.10.1 Core Selection	90
2.3.10.2 Primary Turns Calculation	90
2.3.10.3 Secondary Turns Calculation	91

---

2.3.10.4 Primary rms Current and Wire Size Selection	91
2.3.10.5 Secondary rms Current and Wire Size Selection	92
2.3.10.6 Reset Winding rms Current and Wire Size Selection	92
2.3.11 Output Filter Design Relations	93
2.3.11.1 Output Inductor Design	93
2.3.11.2 Output Capacitor Design	94
2.4 Double-Ended Forward Converter Topology	94
2.4.1 Basic Operation	94
2.4.1.1 Practical Output Power Limits	96
2.4.2 Design Relations and Transformer Design	97
2.4.2.1 Core Selection—Primary Turns and Wire Size	97
2.4.2.2 Secondary Turns and Wire Size	98
2.4.2.3 Output Filter Design	98
2.5 Interleaved Forward Converter Topology	98
2.5.1 Basic Operation—Merits, Drawbacks, and Output Power Limits	98
2.5.2 Transformer Design Relations	100
2.5.2.1 Core Selection	100
2.5.2.2 Primary Turns and Wire Size	100
2.5.2.3 Secondary Turns and Wire Size	101
2.5.3 Output Filter Design	101
2.5.3.1 Output Inductor Design	101
2.5.3.2 Output Capacitor Design	101
Reference	101
<b>3 Half- and Full-Bridge Converter Topologies</b>	<b>103</b>
3.1 Introduction	103
3.2 Half-Bridge Converter Topology	103
3.2.1 Basic Operation	103
3.2.2 Half-Bridge Magnetics	105
3.2.2.1 Selecting Maximum “On” Time, Magnetic Core, and Primary Turns	105
3.2.2.2 The Relation Between Input Voltage, Primary Current, and Output Power	106
3.2.2.3 Primary Wire Size Selection	106
3.2.2.4 Secondary Turns and Wire Size Selection	107
3.2.3 Output Filter Calculations	107
3.2.4 Blocking Capacitor to Avoid Flux Imbalance	107
3.2.5 Half-Bridge Leakage Inductance Problems	109

---

3.2.6 Double-Ended Forward Converter vs. Half Bridge	109
3.2.7 Practical Output Power Limits in Half Bridge	111
3.3 Full-Bridge Converter Topology	111
3.3.1 Basic Operation	111
3.3.2 Full-Bridge Magnetics	113
3.3.2.1 Maximum “On” Time, Core, and Primary Turns Selection	113
3.3.2.2 Relation Between Input Voltage, Primary Current, and Output Power	114
3.3.2.3 Primary Wire Size Selection	114
3.3.2.4 Secondary Turns and Wire Size	114
3.3.3 Output Filter Calculations	115
3.3.4 Transformer Primary Blocking Capacitor	115
<b>4 Flyback Converter Topologies</b>	<b>117</b>
4.1 Introduction	120
4.2 Basic Flyback Converter Schematic	121
4.3 Operating Modes	121
4.4 Discontinuous-Mode Operation	123
4.4.1 Relationship Between Output Voltage, Input Voltage, “On” Time, and Output Load	124
4.4.2 Discontinuous-Mode to Continuous-Mode Transition	124
4.4.3 Continuous-Mode Flyback—Basic Operation	127
4.5 Design Relations and Sequential Design Steps	130
4.5.1 Step 1: Establish the Primary/Secondary Turns Ratio	130
4.5.2 Step 2: Ensure the Core Does Not Saturate and the Mode Remains Discontinuous	130
4.5.3 Step 3: Adjust the Primary Inductance Versus Minimum Output Resistance and DC Input Voltage	131
4.5.4 Step 4: Check Transistor Peak Current and Maximum Voltage Stress	131
4.5.5 Step 5: Check Primary RMS Current and Establish Wire Size	132
4.5.6 Step 6: Check Secondary RMS Current and Select Wire Size	132
4.6 Design Example for a Discontinuous-Mode Flyback Converter	132
4.6.1 Flyback Magnetics	135
4.6.2 Gapping Ferrite Cores to Avoid Saturation	137

---

---

4.6.3 Using Powdered Permalloy (MPP) Cores to Avoid Saturation	138
4.6.4 Flyback Disadvantages	145
4.6.4.1 Large Output Voltage Spikes	145
4.6.4.2 Large Output Filter Capacitor and High Ripple Current Requirement	146
4.7 Universal Input Flybacks for 120-V AC Through 220-V AC Operation	147
4.8 Design Relations—Continuous-Mode Flybacks	149
4.8.1 The Relation Between Output Voltage and “On” Time	149
4.8.2 Input, Output Current – Power Relations	150
4.8.3 Ramp Amplitudes for Continuous Mode at Minimum DC Input	152
4.8.4 Discontinuous- and Continuous-Mode Flyback Design Example	153
4.9 Interleaved Flybacks	155
4.9.1 Summation of Secondary Currents in Interleaved Flybacks	156
4.10 Double-Ended (Two Transistor) Discontinuous-Mode Flyback	157
4.10.1 Area of Application	157
4.10.2 Basic Operation	157
4.10.3 Leakage Inductance Effect in Double-Ended Flyback	159
References	160
<b>5 Current-Mode and Current-Fed Topologies</b>	<b>161</b>
5.1 Introduction	161
5.1.1 Current-Mode Control	161
5.1.2 Current-Fed Topology	162
5.2 Current-Mode Control	162
5.2.1 Current-Mode Control Advantages	163
5.2.1.1 Avoidance of Flux Imbalance in Push-Pull Converters	163
5.2.1.2 Fast Correction Against Line Voltage Changes Without Error Amplifier Delay (Voltage Feed-Forward)	163
5.2.1.3 Ease and Simplicity of Feedback-Loop Stabilization	164
5.2.1.4 Paralleling Outputs	164
5.2.1.5 Improved Load Current Regulation	164
5.3 Current-Mode vs. Voltage-Mode Control Circuits	165
5.3.1 Voltage-Mode Control Circuitry	165
5.3.2 Current-Mode Control Circuitry	169

---

---

5.4 Detailed Explanation of Current-Mode Advantages	171
5.4.1 Line Voltage Regulation	171
5.4.2 Elimination of Flux Imbalance	172
5.4.3 Simplified Loop Stabilization from Elimination of Output Inductor in Small-Signal Analysis	172
5.4.4 Load Current Regulation	174
5.5 Current-Mode Deficiencies and Limitations	176
5.5.1 Constant Peak Current vs. Average Output Current Ratio Problem	176
5.5.2 Response to an Output Inductor Current Disturbance	179
5.5.3 Slope Compensation to Correct Problems in Current Mode	179
5.5.4 Slope (Ramp) Compensation with a Positive-Going Ramp Voltage	181
5.5.5 Implementing Slope Compensation	182
5.6 Comparing the Properties of Voltage-Fed and Current-Fed Topologies	183
5.6.1 Introduction and Definitions	183
5.6.2 Deficiencies of Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge	184
5.6.2.1 Output Inductor Problems in Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge	185
5.6.2.2 Turn “On” Transient Problems in Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge	186
5.6.2.3 Turn “Off” Transient Problems in Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge	187
5.6.2.4 Flux-Imbalance Problem in Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge	188
5.6.3 Buck Voltage-Fed Full-Wave Bridge Topology—Basic Operation	188
5.6.4 Buck Voltage-Fed Full-Wave Bridge Advantages	190
5.6.4.1 Elimination of Output Inductors	190
5.6.4.2 Elimination of Bridge Transistor Turn “On” Transients	191
5.6.4.3 Decrease of Bridge Transistor Turn “Off” Dissipation	192
5.6.4.4 Flux-Imbalance Problem in Bridge Transformer	192

---

---

5.6.5 Drawbacks in Buck Voltage-Fed Full-Wave Bridge	193
5.6.6 Buck Current-Fed Full-Wave Bridge Topology—Basic Operation	193
5.6.6.1 Alleviation of Turn “On” – Turn “Off” Transient Problems in Buck Current-Fed Bridge	195
5.6.6.2 Absence of Simultaneous Conduction Problem in the Buck Current-Fed Bridge	198
5.6.6.3 Turn “On” Problems in Buck Transistor of Buck Current- or Buck Voltage-Fed Bridge	198
5.6.6.4 Buck Transistor Turn “On” Snubber—Basic Operation	201
5.6.6.5 Selection of Buck Turn “On” Snubber Components	202
5.6.6.6 Dissipation in Buck Transistor Snubber Resistor	203
5.6.6.7 Snubbing Inductor Charging Time	203
5.6.6.8 Lossless Turn “On” Snubber for Buck Transistor	204
5.6.6.9 Design Decisions in Buck Current-Fed Bridge	205
5.6.6.10 Operating Frequencies—Buck and Bridge Transistors	206
5.6.6.11 Buck Current-Fed Push-Pull Topology	206
5.6.7 Flyback Current-Fed Push-Pull Topology (Weinberg Circuit)	208
5.6.7.1 Absence of Flux-Imbalance Problem in Flyback Current-Fed Push-Pull Topology	210
5.6.7.2 Decreased Push-Pull Transistor Current in Flyback Current-Fed Topology	211
5.6.7.3 Non-Overlapping Mode in Flyback Current-Fed Push-Pull Topology—Basic Operation	212
5.6.7.4 Output Voltage vs. “On” Time in Non-Overlapping Mode of Flyback Current-Fed Push-Pull Topology	213
5.6.7.5 Output Voltage Ripple and Input Current Ripple in Non-Overlapping Mode	214
5.6.7.6 Output Stage and Transformer Design Example—Non-Overlapping Mode	215

---



---

5.6.7.7 Flyback Transformer for Design Example of Section 5.6.7.6	218
5.6.7.8 Overlapping Mode in Flyback Current-Fed Push-Pull Topology— Basic Operation	219
5.6.7.9 Output/Input Voltages vs. “On” Time in Overlapping Mode	221
5.6.7.10 Turns Ratio Selection in Overlapping Mode	222
5.6.7.11 Output/Input Voltages vs. “On” Time for Overlap-Mode Design at High DC Input Voltages, with Forced Non-Overlap Operation	223
5.6.7.12 Design Example—Overlap Mode	224
5.6.7.13 Voltages, Currents, and Wire Size Selection for Overlap Mode	226
References	227
<b>6 Miscellaneous Topologies</b>	<b>229</b>
6.1 SCR Resonant Topologies—Introduction	229
6.2 SCR and ASCR Basics	231
6.3 SCR Turn “Off” by Resonant Sinusoidal Anode Current—Single-Ended Resonant Inverter Topology	235
6.4 SCR Resonant Bridge Topologies—Introduction	240
6.4.1 Series-Loaded SCR Half-Bridge Resonant Converter—Basic Operation	241
6.4.2 Design Calculations—Series-Loaded SCR Half-Bridge Resonant Converter	245
6.4.3 Design Example—Series-Loaded SCR Half-Bridge Resonant Converter	247
6.4.4 Shunt-Loaded SCR Half-Bridge Resonant Converter	248
6.4.5 Single-Ended SCR Resonant Converter Topology Design	249
6.4.5.1 Minimum Trigger Period Selection	251
6.4.5.2 Peak SCR Current Choice and $LC$ Component Selection	252
6.4.5.3 Design Example	253
6.5 Cuk Converter Topology—Introduction	254
6.5.1 Cuk Converter—Basic Operation	255
6.5.2 Relation Between Output and Input Voltages, and $Q1$ “On” Time	256
6.5.3 Rates of Change of Current in $L1$ , $L2$	257
6.5.4 Reducing Input Ripple Currents to Zero	258
6.5.5 Isolated Outputs in the Cuk Converter	259

---

6.6 Low Output Power “Housekeeping” or “Auxiliary” Topologies— Introduction	260
6.6.1 Housekeeping Power Supply—on Output or Input Common?	261
6.6.2 Housekeeping Supply Alternatives	262
6.6.3 Specific Housekeeping Supply Block Diagrams	262
6.6.3.1 Housekeeping Supply for AC Prime Power	262
6.6.3.2 Oscillator-Type Housekeeping Supply for AC Prime Power	264
6.6.3.3 Flyback-Type Housekeeping Supplies for DC Prime Power	265
6.6.4 Royer Oscillator Housekeeping Supply—Basic Operation	266
6.6.4.1 Royer Oscillator Drawbacks	268
6.6.4.2 Current-Fed Royer Oscillator	271
6.6.4.3 Buck Preregulated Current-Fed Royer Converter	271
6.6.4.4 Square Hysteresis Loop Materials for Royer Oscillators	274
6.6.4.5 Future Potential for Current-Fed Royer and Buck Preregulated Current-Fed Royer	277
6.6.5 Minimum-Parts-Count Flyback as Housekeeping Supply	278
6.6.6 Buck Regulator with DC-Isolated Output as a Housekeeping Supply	280
References	280

## **Part II Magnetics and Circuit Design**

<b>7 Transformers and Magnetic Design</b>	<b>285</b>
7.1 Introduction	285
7.2 Transformer Core Materials and Geometries and Peak Flux Density Selection	286
7.2.1 Ferrite Core Losses versus Frequency and Flux Density for Widely Used Core Materials	286
7.2.2 Ferrite Core Geometries	289
7.2.3 Peak Flux Density Selection	294
7.3 Maximum Core Output Power, Peak Flux Density, Core and Bobbin Areas, and Coil Current Density	295
7.3.1 Derivation of Output Power Relations for Converter Topology	295

---

---

7.3.2 Derivation of Output Power Relations for Push-Pull Topology	299
7.3.2.1 Core and Copper Losses in Push-Pull, Forward Converter Topologies	301
7.3.2.2 Doubling Output Power from a Given Core Without Resorting to a Push-Pull Topology	302
7.3.3 Derivation of Output Power Relations for Half Bridge Topology	304
7.3.4 Output Power Relations in Full Bridge Topology	306
7.3.5 Conversion of Output Power Equations into Charts Permitting Core and Operating Frequency Selection at a Glance	306
7.3.5.1 Peak Flux Density Selection at Higher Frequencies	314
7.4 Transformer Temperature Rise Calculations	315
7.5 Transformer Copper Losses	320
7.5.1 Introduction	320
7.5.2 Skin Effect	321
7.5.3 Skin Effect—Quantitative Relations	323
7.5.4 AC/DC Resistance Ratio for Various Wire Sizes at Various Frequencies	324
7.5.5 Skin Effect with Rectangular Current Waveshapes	327
7.5.6 Proximity Effect	328
7.5.6.1 Mechanism of Proximity Effect	328
7.5.6.2 Proximity Effect Between Adjacent Layers in a Transformer Coil	330
7.5.6.3 Proximity Effect AC/DC Resistance Ratios from Dowell Curves	333
7.6 Introduction: Inductor and Magnetics Design Using the Area Product Method	338
7.6.1 The Area Product Figure of Merit	339
7.6.2 Inductor Design	340
7.6.3 Low Power Signal-Level Inductors	340
7.6.4 Line Filter Inductors	341
7.6.4.1 Common-Mode Line Filter Inductors	341
7.6.4.2 Toroidal Core Common-Mode Line Filter Inductors	341
7.6.4.3 E Core Common-Mode Line Filter Inductors	344
7.6.5 Design Example: Common-Mode 60 Hz Line Filter	345

---

---

7.6.5.1 Step 1: Select Core Size and Establish Area Product	345
7.6.5.2 Step 2: Establish Thermal Resistance and Internal Dissipation Limit	347
7.6.5.3 Step 3: Establish Winding Resistance	348
7.6.5.4 Step 4: Establish Turns and Wire Gauge from the Nomogram Shown in Figure 7.15	349
7.6.5.5 Step 5: Calculating Turns and Wire Gauge	349
7.6.6 Series-Mode Line Filter Inductors	352
7.6.6.1 Ferrite and Iron Powder Rod Core Inductors	353
7.6.6.2 High-Frequency Performance of Rod Core Inductors	355
7.6.6.3 Calculating Inductance of Rod Core Inductors	356
7.7 Magnetics: Introduction to Chokes—Inductors with Large DC Bias Current	358
7.7.1 Equations, Units, and Charts	359
7.7.2 Magnetization Characteristics (B/H Loop) with DC Bias Current	359
7.7.3 Magnetizing Force $H_{dc}$	361
7.7.4 Methods of Increasing Choke Inductance or Bias Current Rating	362
7.7.5 Flux Density Swing $\Delta B$	363
7.7.6 Air Gap Function	366
7.7.7 Temperature Rise	367
7.8 Magnetics Design: Materials for Chokes—Introduction	367
7.8.1 Choke Materials for Low AC Stress Applications	368
7.8.2 Choke Materials for High AC Stress Applications	368
7.8.3 Choke Materials for Mid-Range Applications	369
7.8.4 Core Material Saturation Characteristics	369
7.8.5 Core Material Loss Characteristics	370
7.8.6 Material Saturation Characteristics	371
7.8.7 Material Permeability Parameters	371
7.8.8 Material Cost	373
7.8.9 Establishing Optimum Core Size and Shape	374
7.8.10 Conclusions on Core Material Selection	374
7.9 Magnetics: Choke Design Examples	375
7.9.1 Choke Design Example: Gapped Ferrite E Core	375

---

---

7.9.2 Step 1: Establish Inductance for 20% Ripple Current	376
7.9.3 Step 2: Establish Area Product (AP)	377
7.9.4 Step 3: Calculate Minimum Turns	378
7.9.5 Step 4: Calculate Core Gap	378
7.9.6 Step 5: Establish Optimum Wire Size	380
7.9.7 Step 6: Calculating Optimum Wire Size	381
7.9.8 Step 7: Calculate Winding Resistance	382
7.9.9 Step 8: Establish Power Loss	382
7.9.10 Step 9: Predict Temperature Rise—Area Product Method	383
7.9.11 Step 10: Check Core Loss	383
7.10 Magnetics: Choke Designs Using Powder Core Materials—Introduction	387
7.10.1 Factors Controlling Choice of Powder Core Material	388
7.10.2 Powder Core Saturation Properties	388
7.10.3 Powder Core Material Loss Properties	389
7.10.4 Copper Loss – Limited Choke Designs for Low AC Stress	391
7.10.5 Core Loss – Limited Choke Designs for High AC Stress	392
7.10.6 Choke Designs for Medium AC Stress	392
7.10.7 Core Material Saturation Properties	393
7.10.8 Core Geometry	393
7.10.9 Material Cost	394
7.11 Choke Design Example: Copper Loss Limited Using Kool M $\mu$ Powder Toroid	395
7.11.1 Introduction	395
7.11.2 Selecting Core Size by Energy Storage and Area Product Methods	395
7.11.3 Copper Loss – Limited Choke Design Example	397
7.11.3.1 Step 1: Calculate Energy Storage Number	397
7.11.3.2 Step 2: Establish Area Product and Select Core Size	397
7.11.3.3 Step 3: Calculate Initial Turns	397
7.11.3.4 Step 4: Calculate DC Magnetizing Force	399
7.11.3.5 Step 5: Establish New Relative Permeability and Adjust Turns	399
7.11.3.6 Step 6: Establish Wire Size	399
7.11.3.7 Step 7: Establish Copper Loss	400
7.11.3.8 Step 8: Check Temperature Rise by Energy Density Method	400

---

---

7.11.3.9 Step 9: Predict Temperature Rise by Area Product Method	401
7.11.3.10 Step 10: Establish Core Loss	401
7.12 Choke Design Examples Using Various Powder E Cores	403
7.12.1 Introduction	403
7.12.2 First Example: Choke Using a #40 Iron Powder E Core	404
7.12.2.1 Step 1: Calculate Inductance for 1.5 Amps Ripple Current	404
7.12.2.2 Step 2: Calculate Energy Storage Number	406
7.12.2.3 Step 3: Establish Area Product and Select Core Size	407
7.12.2.4 Step 4: Calculate Initial Turns	407
7.12.2.5 Step 5: Calculate Core Loss	409
7.12.2.6 Step 6: Establish Wire Size	411
7.12.2.7 Step 7: Establish Copper Loss	411
7.12.3 Second Example: Choke Using a #8 Iron Powder E Core	412
7.12.3.1 Step 1: Calculate New Turns	412
7.12.3.2 Step 2: Calculate Core Loss with #8 Mix	412
7.12.3.3 Step 3: Establish Copper Loss	413
7.12.3.4 Step 4: Calculate Efficiency and Temperature Rise	413
7.12.4 Third Example: Choke Using #60 Kool M $\mu$ E Cores	413
7.12.4.1 Step 1: Select Core Size	414
7.12.4.2 Step 2: Calculate Turns	414
7.12.4.3 Step 3: Calculate DC Magnetizing Force	415
7.12.4.4 Step 4: Establish Relative Permeability and Adjust Turns	415
7.12.4.5 Step 5: Calculate Core Loss with #60 Kool M $\mu$ Mix	415
7.12.4.6 Step 6: Establish Wire Size	416
7.12.4.7 Step 7: Establish Copper Loss	416
7.12.4.8 Step 8: Establish Temperature Rise	416
7.13 Swinging Choke Design Example: Copper Loss Limited Using Kool M $\mu$ Powder E Core	417
7.13.1 Swinging Chokes	417
7.13.2 Swinging Choke Design Example	418
7.13.2.1 Step 1: Calculate Energy Storage Number	418

---

7.13.2.2 Step 2: Establish Area Product and Select Core Size	418
7.13.2.3 Step 3: Calculate Turns for 100 Oersteds	419
7.13.2.4 Step 4: Calculate Inductance	419
7.13.2.5 Step 5: Calculate Wire Size	420
7.13.2.6 Step 6: Establish Copper Loss	420
7.13.2.7 Step 7: Check Temperature Rise by Thermal Resistance Method	420
7.13.2.8 Step 8: Establish Core Loss	421
References	421
<b>8 Bipolar Power Transistor Base Drive Circuits</b>	<b>423</b>
8.1 Introduction	423
8.2 The Key Objectives of Good Base Drive Circuits for Bipolar Transistors	424
8.2.1 Sufficiently High Current Throughout the “On” Time	424
8.2.2 A Spike of High Base Input Current $I_{b1}$ at Instant of Turn “On”	425
8.2.3 A Spike of High Reverse Base Current $I_{b2}$ at the Instant of Turn “Off”	427
(Figure 8.2a)	
8.2.4 A Base-to-Emitter Reverse Voltage Spike $-1$ to $-5$ V in Amplitude at the Instant of Turn “Off”	427
8.2.5 The Baker Clamp (A Circuit That Works Equally Well with High-or Low-Beta Transistors)	429
8.2.6 Improving Drive Efficiency	429
8.3 Transformer Coupled Baker Clamp Circuits	430
8.3.1 Baker Clamp Operation	431
8.3.2 Transformer Coupling into a Baker Clamp	435
8.3.2.1 Transformer Supply Voltage, Turns Ratio Selection, and Primary and Secondary Current Limiting	435
8.3.2.2 Power Transistor Reverse Base Current Derived from Flyback Action in Drive Transformer	437
8.3.2.3 Drive Transformer Primary Current Limiting to Achieve Equal Forward and Reverse Base Currents in Power Transistor at End of the “On” Time	438
8.3.2.4 Design Example—Transformer-Driven Baker Clamp	439

8.3.3 Baker Clamp with Integral Transformer	440
8.3.3.1 Design Example—Transformer Baker Clamp	442
8.3.4 Inherent Baker Clamping with a Darlington Transistor	442
8.3.5 Proportional Base Drive	443
8.3.5.1 Detailed Circuit Operation—Proportional Base Drive	443
8.3.5.2 Quantitative Design of Proportional Base Drive Scheme	446
8.3.5.3 Selection of Holdup Capacitor ( $C_1$ , Figure 8.12) to Guarantee Power Transistor Turn “Off”	447
8.3.5.4 Base Drive Transformer Primary Inductance and Core Selection	449
8.3.5.5 Design Example—Proportional Base Drive	449
8.3.6 Miscellaneous Base Drive Schemes	450
References	455
<b>9 MOSFET and IGBT Power Transistors and Gate Drive Requirements</b>	<b>457</b>
9.1 MOSFET Introduction	457
9.1.1 IGBT Introduction	457
9.1.2 The Changing Industry	458
9.1.3 The Impact on New Designs	458
9.2 MOSFET Basics	459
9.2.1 Typical Drain Current vs. Drain-to-Source Voltage Characteristics ( $I_d$ — $V_{ds}$ ) for a FET Device	461
9.2.2 “On” State Resistance $r_{ds}$ (on)	461
9.2.3 MOSFET Input Impedance Miller Effect and Required Gate Currents	464
9.2.4 Calculating the Gate Voltage Rise and Fall Times for a Desired Drain Current Rise and Fall Time	467
9.2.5 MOSFET Gate Drive Circuits	468
9.2.6 MOSFET $R_{ds}$ Temperature Characteristics and Safe Operating Area	473
Limits	
9.2.7 MOSFET Gate Threshold Voltage and Temperature Characteristics	475
9.2.8 MOSFET Switching Speed and Temperature Characteristics	476
9.2.9 MOSFET Current Ratings	477
9.2.10 Paralleling MOSFETs	480
9.2.11 MOSFETs in Push-Pull Topology	483
9.2.12 MOSFET Maximum Gate Voltage Specifications	484
9.2.13 MOSFET Drain-to-Source “Body” Diode	485



---

9.3 Introduction to Insulated Gate Bipolar Transistors (IGBTs)	487
9.3.1 Selecting Suitable IGBTs for Your Application	488
9.3.2 IGBT Construction Overview	489
9.3.2.1 Equivalent Circuits	490
9.3.3 Performance Characteristics of IGBTs	490
9.3.3.1 Turn “Off” Characteristics of IGBTs	490
9.3.3.2 The Difference Between PT- and NPT-Type IGBTs	491
9.3.3.3 The Conduction of PT- and NPT-Type IGBTs	491
9.3.3.4 The Link Between Ruggedness and Switching Loss in PT- and NPT-Type IGBTs	491
9.3.3.5 IGBT Latch-Up Possibilities	492
9.3.3.6 Temperature Effects	493
9.3.4 Parallel Operation of IGBTs	493
9.3.5 Specification Parameters and Maximum Ratings	494
9.3.6 Static Electrical Characteristics	498
9.3.7 Dynamic Characteristics	499
9.3.8 Thermal and Mechanical Characteristics	504
References	509
<b>10 Magnetic-Amplifier Postregulators</b>	<b>511</b>
10.1 Introduction	511
10.2 Linear and Buck Postregulators	513
10.3 Magnetic Amplifiers—Introduction	513
10.3.1 Square Hysteresis Loop Magnetic Core as a Fast Acting On/Off Switch with Electrically Adjustable “On” and “Off” Times	516
10.3.2 Blocking and Firing Times in Magnetic-Amplifier Postregulators	519
10.3.3 Magnetic-Amplifier Core Resetting and Voltage Regulation	520
10.3.4 Slave Output Voltage Shutdown with Magnetic Amplifiers	521
10.3.5 Square Hysteresis Loop Core Characteristics and Sources	522
10.3.6 Core Loss and Temperature Rise Calculations	529
10.3.7 Design Example—Magnetic-Amplifier Postregulator	534

---

---

10.3.8 Magnetic-Amplifier Gain	539
10.3.9 Magnetic Amplifiers for a Push-Pull Output	540
10.4 Magnetic Amplifier Pulse-Width Modulator and Error Amplifier	540
10.4.1 Circuit Details, Magnetic Amplifier Pulse-Width Modulator – Error Amplifier	541
References	544
<b>11 Analysis of Turn “On” and Turn “Off” Switching Losses and the Design of Load-Line Shaping Snubber Circuits</b>	<b>545</b>
11.1 Introduction	545
11.2 Transistor Turn “Off” Losses Without a Snubber	547
11.3 RCD Turn “Off” Snubber Operation	548
11.4 Selection of Capacitor Size in <i>RCD</i> Snubber	550
11.5 Design Example— <i>RCD</i> Snubber	551
11.5.1 <i>RCD</i> Snubber Returned to Positive Supply Rail	552
11.6 Non-Dissipative Snubbers	553
11.7 Load-Line Shaping (The Snubber’s Ability to Reduce Spike Voltages so as to Avoid Secondary Breakdown)	555
11.8 Transformer Lossless Snubber Circuit	558
References	559
<b>12 Feedback Loop Stabilization</b>	<b>561</b>
12.1 Introduction	561
12.2 Mechanism of Loop Oscillation	563
12.2.1 The Gain Criterion for a Stable Circuit	563
12.2.2 Gain Slope Criteria for a Stable Circuit	563
12.2.3 Gain Characteristic of Output <i>LC</i> Filter with and without Equivalent Series Resistance (ESR) in Output Capacitor	567
12.2.4 Pulse-Width-Modulator Gain	570
12.2.5 Gain of Output <i>LC</i> Filter Plus Modulator and Sampling Network	571
12.3 Shaping Error-Amplifier Gain Versus Frequency Characteristic	572
12.4 Error-Amplifier Transfer Function, Poles, and Zeros	575
12.5 Rules for Gain Slope Changes Due to Zeros and Poles	576

---

12.6 Derivation of Transfer Function of an Error Amplifier with Single Zero and Single Pole from Its Schematic	578
12.7 Calculation of Type 2 Error-Amplifier Phase Shift from Its Zero and Pole Locations	579
12.8 Phase Shift Through <i>LC</i> Filter with Significant ESR	580
12.9 Design Example—Stabilizing a Forward Converter Feedback Loop with a Type 2 Error Amplifier	582
12.10 Type 3 Error Amplifier—Application and Transfer Function	585
12.11 Phase Lag Through a Type 3 Error Amplifier as Function of Zero and Pole Locations	587
12.12 Type 3 Error Amplifier Schematic, Transfer Function, and Zero and Pole Locations	588
12.13 Design Example—Stabilizing a Forward Converter Feedback Loop with a Type 3 Error Amplifier	590
12.14 Component Selection to Yield Desired Type 3 Error-Amplifier Gain Curve	592
12.15 Conditional Stability in Feedback Loops	593
12.16 Stabilizing a Discontinuous-Mode Flyback Converter	595
12.16.1 DC Gain from Error-Amplifier Output to Output Voltage Node	595
12.16.2 Discontinuous-Mode Flyback Transfer Function from Error-Amplifier Output to Output Voltage Node	597
12.17 Error-Amplifier Transfer Function for Discontinuous-Mode Flyback	599
12.18 Design Example—Stabilizing a Discontinuous-Mode Flyback Converter	600
12.19 Transconductance Error Amplifiers	602
References	605
<b>13 Resonant Converters</b>	<b>607</b>
13.1 Introduction	607
13.2 Resonant Converters	608
13.3 The Resonant Forward Converter	609
13.3.1 Measured Waveforms in a Resonant Forward Converter	612
13.4 Resonant Converter Operating Modes	614
13.4.1 Discontinuous and Continuous: Operating Modes Above and Below Resonance	614

---

13.5 Resonant Half Bridge in Continuous-Conduction Mode	616
13.5.1 Parallel Resonant Converter (PRC) and Series Resonant Converter (SRC)	616
13.5.2 AC Equivalent Circuits and Gain Curves for Series-Loaded and Parallel-Loaded Half Bridges Operating in the Continuous-Conduction Mode	619
13.5.3 Regulation with Series-Loaded Half Bridge in Continuous-Conduction Mode (CCM)	620
13.5.4 Regulation with a Parallel-Loaded Half Bridge in the Continuous-Conduction Mode	621
13.5.5 Series-Parallel Resonant Converter in Continuous-Conduction Mode	622
13.5.6 Zero-Voltage-Switching Quasi-Resonant (CCM) Converters	623
13.6 Resonant Power Supplies—Conclusion	627
References	628

### Part III Waveforms

<b>14 Typical Waveforms for Switching Power Supplies</b>	<b>631</b>
14.1 Introduction	631
14.2 Forward Converter Waveshapes	632
14.2.1 $V_{ds}$ , $I_d$ Photos at 80% of Full Load	633
14.2.2 $V_{ds}$ , $I_d$ Photos at 40% of Full Load	635
14.2.3 Overlap of Drain Voltage and Drain Current at Turn “On” /Turn “Off” Transitions	635
14.2.4 Relative Timing of Drain Current, Drain-to-Source Voltage, and Gate-to-Source Voltage	638
14.2.5 Relationship of Input Voltage to Output Inductor, Output Inductor Current Rise and Fall Times, and Power Transistor Drain-Source Voltage	638
14.2.6 Relative Timing of Critical Waveforms in PWM Driver Chip (UC3525A) for Forward Converter of Figure 14.1	639
14.3 Push-Pull Topology Waveshapes—Introduction	640
14.3.1 Transformer Center Tap Currents and Drain-to-Source Voltages at Maximum Load Currents for Maximum, Nominal, and Minimum Supply Voltages	642

---

14.3.2 Opposing $V_{ds}$ Waveshapes, Relative Timing, and Flux Locus During Dead Time	644
14.3.3 Relative Timing of Gate Input Voltage, Drain-to-Source Voltage, and Drain Currents	647
14.3.4 Drain Current Measured with a Current Probe in the Drain Compared to that Measured with a Current Probe in the Transformer Center Tap	647
14.3.5 Output Ripple Voltage and Rectifier Cathode Voltage	647
14.3.6 Oscillatory Ringing at Rectifier Cathodes after Transistor Turn “On”	650
14.3.7 AC Switching Loss Due to Overlap of Falling Drain Current and Rising Drain Voltage at Turn “Off”	650
14.3.8 Drain Currents as Measured in the Transformer Center Tap and Drain-to-Source Voltage at One-Fifth of Maximum Output Power	652
14.3.9 Drain Current and Voltage at One-Fifth Maximum Output Power	655
14.3.10 Relative Timing of Opposing Drain Voltages at One-Fifth Maximum Output Currents	655
14.3.11 Controlled Output Inductor Current and Rectifier Cathode Voltage	656
14.3.12 Controlled Rectifier Cathode Voltage Above Minimum Output Current	656
14.3.13 Gate Voltage and Drain Current Timing	656
14.3.14 Rectifier Diode and Transformer Secondary Currents	656
14.3.15 Apparent Double Turn “On” per Half Period Arising from Excessive Magnetizing Current or Insufficient Output Currents	658
14.3.16 Drain Currents and Voltages at 15% Above Specified Maximum Output Power	659
14.3.17 Ringing at Drain During Transistor Dead Time	659
14.4 Flyback Topology Waveshapes	660
14.4.1 Introduction	660
14.4.2 Drain Current and Voltage Waveshapes at 90% of Full Load for Minimum, Nominal, and Maximum Input Voltages	662
14.4.3 Voltage and Currents at Output Rectifier Inputs	662

---

14.4.4 Snubber Capacitor Current at Transistor Turn “Off”	665
References	666

## **Part IV More Recent Applications for Switching Power Supply Techniques**

<b>15 Power Factor and Power Factor Correction</b>	<b>669</b>
15.1 Power Factor—What Is It and Why Must It Be Corrected?	669
15.2 Power Factor Correction in Switching Power Supplies	671
15.3 Power Factor Correction—Basic Circuit Details	673
15.3.1 Continuous- Versus Discontinuous-Mode Boost Topology for Power Factor Correction	676
15.3.2 Line Input Voltage Regulation in Continuous-Mode Boost Converters	678
15.3.3 Load Current Regulation in Continuous-Mode Boost Regulators	679
15.4 Integrated-Circuit Chips for Power Factor Correction	681
15.4.1 The Unitrode UC 3854 Power Factor Correction Chip	681
15.4.2 Forcing Sinusoidal Line Current with the UC 3854	682
15.4.3 Maintaining Constant Output Voltage with UC 3854	684
15.4.4 Controlling Power Output with the UC 3854	685
15.4.5 Boost Switching Frequency with the UC 3854	687
15.4.6 Selection of Boost Output Inductor $L$	687
15.4.7 Selection of Boost Output Capacitor	688
15.4.8 Peak Current Limiting in the UC 3854	690
15.4.9 Stabilizing the UC 3854 Feedback Loop	690
15.5 The Motorola MC 34261 Power Factor Correction Chip	691
15.5.1 More Details of the Motorola MC 34261 (Figure 15.11)	693
15.5.2 Logic Details for the MC 34261 (Figures 15.11 and 15.12)	693
15.5.3 Calculations for Frequency and Inductor $L$	694
15.5.4 Selection of Sensing and Multiplier Resistors for the MC 34261	696
References	697

---

<b>16 Electronic Ballasts: High-Frequency Power Regulators for Fluorescent Lamps</b>	<b>699</b>
16.1 Introduction: Magnetic Ballasts	699
16.2 Fluorescent Lamp—Physics and Types	703
16.3 Electric Arc Characteristics	706
16.3.1 Arc Characteristics with DC Supply Voltage	707
16.3.2 AC-Driven Fluorescent Lamps	709
16.3.3 Fluorescent Lamp Volt/Ampere Characteristics with an Electronic Ballast	711
16.4 Electronic Ballast Circuits	715
16.5 DC/AC Inverter—General Characteristics	716
16.6 DC/AC Inverter Topologies	717
16.6.1 Current-Fed Push-Pull Topology	718
16.6.2 Voltage and Currents in Current-Fed Push-Pull Topology	720
16.6.3 Magnitude of “Current Feed” Inductor in Current-Fed Topology	721
16.6.4 Specific Core Selection for Current Feed Inductor	722
16.6.5 Coil Design for Current Feed Inductor	729
16.6.6 Ferrite Core Transformer for Current-Fed Topology	729
16.6.7 Toroidal Core Transformer for Current-Fed Topology	737
16.7 Voltage-Fed Push-Pull Topology	737
16.8 Current-Fed Parallel Resonant Half Bridge Topology	740
16.9 Voltage-Fed Series Resonant Half Bridge Topology	742
16.10 Electronic Ballast Packaging	745
References	745
<b>17 Low-Input-Voltage Regulators for Laptop Computers and Portable Electronics</b>	<b>747</b>
17.1 Introduction	747
17.2 Low-Input-Voltage IC Regulator Suppliers	748
17.3 Linear Technology Corporation Boost and Buck Regulators	749
17.3.1 Linear Technology LT1170 Boost Regulator	751
17.3.2 Significant Waveform Photos in the LT1170 Boost Regulator	753
17.3.3 Thermal Considerations in IC Regulators	756

---

---

17.3.4	Alternative Uses for the LT1170 Boost Regulator	759
17.3.4.1	LT1170 Buck Regulator	759
17.3.4.2	LT1170 Driving High-Voltage MOSFETS or NPN Transistors	759
17.3.4.3	LT1170 Negative Buck Regulator	762
17.3.4.4	LT1170 Negative-to-Positive Polarity Inverter	762
17.3.4.5	Positive-to-Negative Polarity Inverter	763
17.3.4.6	LT1170 Negative Boost Regulator	763
17.3.5	Additional LTC High-Power Boost Regulators	763
17.3.6	Component Selection for Boost Regulators	764
17.3.6.1	Output Inductor $L_1$ Selection	764
17.3.6.2	Output Capacitor $C_1$ Selection	765
17.3.6.3	Output Diode Dissipation	767
17.3.7	Linear Technology Buck Regulator Family	767
17.3.7.1	LT1074 Buck Regulator	767
17.3.8	Alternative Uses for the LT1074 Buck Regulator	770
17.3.8.1	LT1074 Positive-to-Negative Polarity Inverter	770
17.3.8.2	LT1074 Negative Boost Regulator	771
17.3.8.3	Thermal Considerations for LT1074	773
17.3.9	LTC High-Efficiency, High-Power Buck Regulators	775
17.3.9.1	LT1376 High-Frequency, Low Switch Drop Buck Regulator	775
17.3.9.2	LTC1148 High-Efficiency Buck with External MOSFET Switches	775
17.3.9.3	LTC1148 Block Diagram	777
17.3.9.4	LTC1148 Line and Load Regulation	780
17.3.9.5	LTC1148 Peak Current and Output Inductor Selection	780
17.3.9.6	LTC1148 Burst-Mode Operation for Low Output Current	781
17.3.10	Summary of High-Power Linear Technology Buck Regulators	782
17.3.11	Linear Technology Micropower Regulators	783
17.3.12	Feedback Loop Stabilization	783

---



---

17.4 Maxim IC Regulators	787
17.5 Distributed Power Systems with IC Building Blocks	787
References	792
<b>Appendix</b>	<b>793</b>
<b>Bibliography</b>	<b>797</b>
<b>Index</b>	<b>807</b>

---



## Acknowledgments

Worthy of special mention is my engineering colleague and friend of many years, Taylor Morey. He spent many more hours than I did carefully checking the text, grammar, figures, diagrams, tables, equations, and formulae in this new edition. I know he made many thousands of adjustments, but should any errors remain they are entirely my responsibility.

I am also indebted to Anne Pressman for permission to work on this edition and to Wendy Rinaldi and LeeAnn Pickrell and the publishing staff of McGraw-Hill for adding the professional touch.

Many people contribute to a work like this, not the least of these being the many authors of the published works mentioned in the bibliography and references. Some who go unnamed also deserve our thanks. “We see further because we stand on the shoulders of giants.”

—Keith Billings

---



## Preface

Not many technical books continue to be in high demand well beyond the natural life of their author. It speaks well to the excellent work done by Abraham Pressman that his book on switching power supply design, first published in 1977, still enjoys brisk sales some eight years after his demise at the age of 86. He leaves us a valuable legacy, well proven by the test of time.

Abraham had been active in the electronics industry for nearly six decades. For 15 years, up to the age of 83, Abraham had presented a training course on switching design. I was privileged to know Abraham and collaborate with him on various projects in his later years. Abe would tell his students that my book was the *second* best book on switching power supplies (not true, but rare and valuable praise indeed from the old master).

When I started designing switching power supplies in the 1960s, very little information on the subject was available. It was a new technology, and the few companies and engineers specializing in this area were not about to tell the rest of world what they were doing. When I found Abraham's book, a veil of secrecy was drawn away, shedding light on this new technology. With the insight provided by Abe, I moved forward with great strides.

When, in 2000, Abe found he was no longer able to continue with his training course, I was proud that he asked me to take over his course notes with a view to continuing his presentation. I found the volume of information to be daunting, however, and too much for me to present in four days, although he had done so for many years. Furthermore, I felt that the notes and overhead slides had deteriorated too much to be easily readable.

I simplified the presentation and converted it to PowerPoint on my laptop, and I first presented the modified, three-day course in Boston in November 2001. There were only two students (most companies had cut back their training budget), but this poor turnout was more than compensated for by the attendance of Abraham and his wife Anne. Abe was very frail by then, and I was so pleased that he lived to see his legacy living on, albeit in a very different form. I think he was a bit bemused by the dynamic multimedia presentation, as I leisurely

---

controlled it from my laptop. I never found out what he really thought about it, but Anne waved a finger and said, “Abe would stand at the blackboard with a pointer to do that!”

When McGraw-Hill asked me to co-author the third edition of Abe’s book, I was pleased to agree, as I believe he would have wanted me to do that. In the eight years since the publication of the second edition, there have been many advances in the technology and vast improvements in the performance of essential components. This has altered many of the limitations that Abe mentions, so this was a good time to make adjustments and add some new work.

As I reviewed the second edition, a comment made by an English gardener standing outside his cottage in a country village unchanged for hundreds of years, came to mind. In response to a new arrival, a young yuppie who wanted to modernize things, he said, “Look around you lad, there’s not much wrong wi’ it, is there?” This comment could well be applied to Abe’s previous edition.

For this reason, I decided not to change Abe’s well-proven treatise, except where technology has overtaken his previous work. His pragmatic approach, dealing with each topology as an independent entity, may not be in the modern idiom as taught by today’s experts, but for the *ab initio* engineer trying to understand the bewildering array of possible topologies, as well as for the more experienced engineer, it is a well-proven and effective method. The state-space averaging models, canonical models, the bilateral inversion techniques, or duality principles so valuable to modern experts in this field were not for Abraham. His book provides a solid underpinning of the fundamentals, explaining not only how but also why we do things. There is time enough later to learn the more modern concepts from some of the excellent specialist books now available (see the bibliography).

Abe’s original manuscript was handwritten and painstakingly typed out by his wife Anne over several years. For this third edition, McGraw-Hill converted the manuscript to digital files for ease of editing. This made it easier for Taylor Morey and me to make minor and mainly cosmetic changes to the text and many corrections to equations, calculations, and diagrams, some corrupted by the conversion process. We also made adjustments where we felt such changes would help the flow, making it easier for the reader to follow the presentation. These changes are transparent to the reader, and they do not change Abraham’s original intentions.

Where new technology and recent improvements in components have changed some of the limitations mentioned in the second edition, you will find my adjusting notes under the heading **After Pressman**. Where I felt additional explanations were justified, I have inserted a **Tip** or **Note**.

---

I have also added new sections to Chapter 7 and Chapter 9, where I felt that recent improvements in design methods would be helpful to the reader and also where improvements in IGBT technology made these devices a useful addition to the more limited range of devices previously favored by Abraham. In this way, the original structure of the second edition remains unchanged, and because the index and cross references still apply, the reader will find favorite sections in the same places. Unfortunately, the page numbers did change, as there was no way to avoid this.

Even if you already have a copy of the second edition of Pressman's book, I am sure that with the improvements and additional sections, you will find the third edition a worthwhile addition to your reference library. You will also find my book, *Switchmode Power Supply Handbook*, Second Edition (McGraw-Hill, 1999), a good companion, providing additional information with a somewhat different approach to the subject.

---

Source: Switching Power Supply Design

# PART 1

---

# Topologies



## Topologies

# CHAPTER 1

---

## Basic Topologies

---

### 1.1 Introduction to Linear Regulators and Switching Regulators of the Buck Boost and Inverting Types

In this book, we describe many well-known *topologies* (elemental building blocks) that are commonly used to implement linear and switching power supply designs. Each topology has both common and unique properties, and the experienced designer will choose the topology best suited for the intended application. However, for those engineers just starting in this area, the choice may appear rather daunting. It is worth spending some time to develop a basic understanding of the properties, because the correct initial choice will avoid wasting time on a topology that may not be the best for the application.

We will see that some topologies are best used for AC/DC offline converters at lower output powers (say,  $< 200\text{ W}$ ), whereas others will be better at higher output powers. Again some will be a better choice for higher AC input voltages (say,  $\geq 220\text{ VAC}$ ), whereas others will be better at lower AC input voltages. In a similar way, some will have advantages for higher DC output voltages (say,  $> 200\text{ V}$ ), yet others are preferred at lower DC voltages. For applications where several output voltages are required, some topologies will have a lower parts count or may offer a trade-off in parts counts versus reliability, while input or output ripple and noise requirements will also be an important factor. Further, some topologies have inherent limitations that require additional or more complex circuitry, whereas the performance of others can become difficult to analyze in some situations.

So we should now see how helpful it can be in our initial design choice to have at least a working knowledge of the merits and limitations of all the basic topologies. A poor initial choice can result in performance limitation and perhaps in extended design time and cost. Hence it is well worth the time and effort to get to know the basic performance parameters of the various topologies.

## 4 Switching Power Supply Design

In this first chapter, we describe some of the earliest and most fundamental building blocks that form the basis of all linear and switching power systems. These include the following regulators:

- Linear regulator
- Buck regulator
- Boost regulator
- Inverting regulator (also known as *flyback* or *buck-boost*)

We describe the basic operation of each type, show and explain the various waveforms, and describe the merits and limitations of each topology. The peak transistor currents and voltage stresses are shown for various output power and input voltage conditions. We look at the dependence of input current on output power and input voltage. We examine efficiency, DC and AC switching losses, and some typical applications.

---

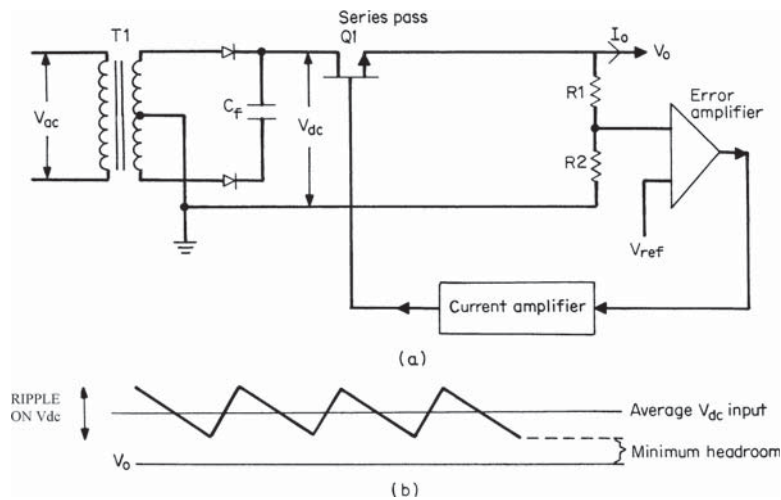
### 1.2 Linear Regulator—the Dissipative Regulator

#### 1.2.1 Basic Operation

To demonstrate the main advantage of the more complex switching regulators, the discussion starts with an examination of the basic properties of what preceded them—the linear or *series-pass* regulator.

Figure 1.1a shows the basic topology of the linear regulator. It consists of a transistor  $Q1$  (operating in the linear, or non-switching mode) to form an electrically variable resistance between the DC source ( $V_{dc}$ ) developed by the 60-Hz isolation transformer, rectifiers, and storage capacitor  $C_f$ , and the output terminal at  $V_o$  that is connected to the external load (not shown).

In Figure 1.1a, an error amplifier senses the DC output voltage  $V_o$  via a sampling resistor network  $R1$ ,  $R2$  and compares it with a reference voltage  $V_{ref}$ . The error amplifier output drives the base of the series-pass power transistor  $Q1$  via a drive circuit. The phasing is such that if the DC output voltage  $V_o$  tends to increase (say, as a result of either an increase in input voltage or a decrease in output load current), the drive to the base of the series-pass transistor is reduced. This increases the resistance of the series-pass element  $Q1$  and hence controls the output voltage so that the sampled output continues to track the reference voltage. This negative-feedback loop works in the reverse direction for any decreases in output voltage, such that the error amplifier increases the drive to  $Q1$  decreasing the collector-to-emitter resistance, thus maintaining the value of  $V_o$  constant.



**FIGURE 1.1** (a) The linear regulator. The waveform shows the ripple normally present on the unregulated DC input ( $V_{dc}$ ). Transistor  $Q_1$ , between the DC source at  $C_f$  and the output load at  $V_o$ , acts as an electrically variable resistance. The negative-feedback loop via the error amplifier alters the effective resistance of  $Q_1$  and will keep  $V_o$  constant, providing the input voltage sufficiently exceeds the output voltage. (b) Figure 1.1b shows the minimum input-output voltage differential (or *headroom*) required in a linear regulator. With a typical NPN series-pass transistor, a minimum input-output voltage differential (headroom) of at least 2.5 V is required between  $V_o$  and the bottom of the  $C_f$  input ripple waveform at minimum  $V_{ac}$  input.

In general, any change in input voltage—due to, for example, AC input line voltage change, ripple, steady-state changes in the input or output, and any dynamic changes resulting from rapid load changes over its designed tolerance band—is absorbed across the series-pass element. This maintains the output voltage constant to an extent determined by the gain in the open-loop feedback amplifier.

Switching regulators have transformers and fast switching actions that can cause considerable RFI noise. However, in the linear regulator the feedback loop is entirely DC-coupled. There are no switching actions within the loop. As a result, all DC voltage levels are predictable and calculable. This lower RFI noise can be a major advantage in some applications, and for this reason, linear regulators still have a place in modern power supply applications even though the efficiency is quite low. Also since the power losses are mainly due to the DC current and the voltage across  $Q_1$ , the loss and the overall efficiency are easily calculated.

## 6 Switching Power Supply Design

### 1.2.2 Some Limitations of the Linear Regulator

This simple, DC-coupled series-pass linear regulator was the basis for a multi-billion-dollar power supply industry until the early 1960s. However, in simple terms, it has the following limitations:

- The linear regulator is constrained to produce only a lower regulated voltage from a higher non-regulated input.
- The output always has one terminal that is common with the input. This can be a problem, complicating the design when DC isolation is required between input and output or between multiple outputs.
- The raw DC input voltage ( $V_{dc}$  in Figure 1.1a) is usually derived from the rectified secondary of a 60-Hz transformer whose weight and volume was often a serious system constraint.
- As shown next, the regulation efficiency is very low, resulting in a considerable power loss needing large heat sinks in relatively large and heavy power units.

### 1.2.3 Power Dissipation in the Series-Pass Transistor

A major limitation of a linear regulator is the inevitable and large dissipation in the series-pass element. It is clear that all the load current must pass through the pass transistor  $Q1$ , and its dissipation will be  $(V_{dc} - V_o)(I_o)$ . The minimum differential ( $V_{dc} - V_o$ ), the headroom, is typically 2.5 V for NPN pass transistors. Assume for now that the filter capacitor is large enough to yield insignificant ripple. Typically the raw DC input comes from the rectified secondary of a 60-Hz transformer. In this case the secondary turns can always be chosen so that the rectified secondary voltage is near  $V_o + 2.5$  V when the input AC is at its low tolerance limit. At this point the dissipation in  $Q1$  will be quite low.

However, when the input AC voltage is at its high tolerance limit, the voltage across  $Q1$  will be much greater, and its dissipation will be larger, reducing the power supply efficiency. Due to the minimum 2.5-volt headroom requirement, this effect is much more pronounced at lower output voltages.

This effect is dramatically demonstrated in the following examples. We will assume an AC input voltage range of  $\pm 15\%$ . Consider three examples as follows:

- Output of 5 V at 10 A
- Output of 15 V at 10 A
- Output of 30 V at 10 A

Assume for now that a large secondary filter capacitor is used such that ripple voltage to the regulator is negligible. The rectified secondary voltage range ( $V_{dc}$ ) will be identical to the AC input voltage range of  $\pm 15\%$ . The transformer secondary voltages will be chosen to yield ( $V_o + 2.5$  V) when the AC input is at its low tolerance limit of  $-15\%$ . Hence, the maximum DC input is 35% higher when the AC input is at its maximum tolerance limit of  $+15\%$ . This yields the following:

$V_o$	$I_o$ , A	$V_{dc(min)}$ V	$V_{dc(max)}$ V	Headroom, max, V	$P_{in(max)}$ W	$P_{out(max)}$ W	Dissipation $Q1_{max}$	Efficiency, % $P_o/P_{in(max)}$
5.0	10	7.5	10.1	5.1	101	50	51	50
15.0	10	17.5	23.7	8.7	237	150	87	63
30.0	10	32.5	44.0	14	440	300	140	68

It is clear from this example that at lower DC output voltages the efficiency will be very low. In fact, as shown next, when realistic input line ripple voltages are included, the efficiency for a 5-volt output with a line voltage range of  $\pm 15\%$  will be only 32 to 35%.

### 1.2.4 Linear Regulator Efficiency vs. Output Voltage

We will consider in general the range of efficiency expected for a range of output voltages from 5 V to 100 V with line inputs ranging from  $\pm 5$  to  $\pm 15\%$  when a realistic ripple value is included.

Assume the minimum headroom is to be 2.5 V, and this must be guaranteed at the bottom of the input ripple waveform at the lower limit of the input AC voltages range, as shown in Figure 1.1b. Regulator efficiency can be calculated as follows for various assumed input AC tolerances and output voltages.

Let the input voltage range be  $\pm T\%$  about its nominal. The transformer secondary turns will be selected so that the voltage at the bottom of the ripple waveform will be 2.5 V above the desired output voltage when the AC input is at its lower limit.

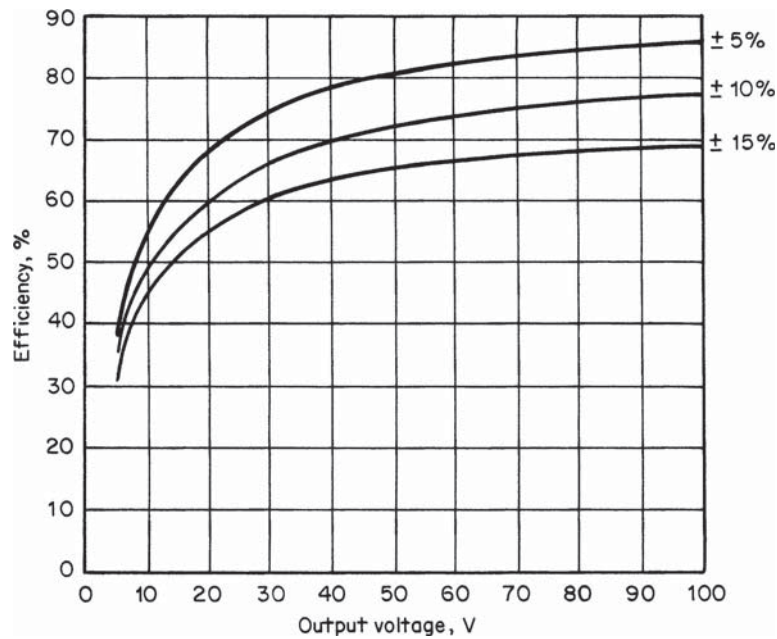
Let the peak-to-peak ripple voltage be  $V_r$  volts. When the input AC is at its low tolerance limit, the average or DC voltage at the input to the pass transistor will be

$$V_{dc} = (V_o + 2.5 + V_r/2) \text{ volts}$$

When the AC input is at its high tolerance limit, the DC voltage at the input to the series-pass element is

$$V_{dc(max)} = \frac{1 + 0.01T}{1 - 0.01T} (V_o + 2.5 + V_r/2)$$

## 8 Switching Power Supply Design



**FIGURE 1.2** Linear regulator efficiency versus output voltage. Efficiency shown for maximum  $V_{ac}$  input, assuming a 2.5-V headroom is maintained at the bottom of the ripple waveform at minimum  $V_{ac}$  input. Eight volts peak-to-peak ripple is assumed at the top of the filter capacitor. (From Eq. 1.2)

The maximum achievable worst-case efficiency (which occurs at maximum input voltage and hence maximum input power) is

$$\text{Efficiency}_{\max} = \frac{P_o}{P_{in(\max)}} = \frac{V_o I_o}{V_{dc(\max)} I_o} = \frac{V_o}{V_{dc(\max)}} \quad (1.1)$$

$$= \frac{1 - 0.01T}{1 + 0.01T} \left( \frac{V_o}{V_o + 2.5 + V_r/2} \right) \quad (1.2)$$

This is plotted in Figure 1.2 for an assumed peak-to-peak (p/p) ripple voltage of 8 V. It will be shown that in a 60-Hz full-wave rectifier, the p/p ripple voltage is 8 V if the filter capacitor is chosen to be of the order of 1000 microfarads ( $\mu\text{F}$ ) per ampere of DC load current, an industry standard value.

It can be seen in Figure 1.2 that even for 10-V outputs, the efficiency is less than 50% for a typical AC line range of  $\pm 10\%$ . In general it is the poor efficiency, the weight, the size, and the cost of the 60-Hz input transformer that was the driving force behind the development of switching power supplies.

However, the linear regulator with its lower electrical noise still has applications and may not have excessive power loss. For example, if a reasonably pre-regulated input is available (frequently the case in some of the switching configurations to be shown later), a linear regulator is a reasonable choice where lower noise is required. Complete integrated-circuit linear regulators are available up to 3-A output in single plastic packages and up to 5 A in metal-case integrated-circuit packages. However, the dissipation across the internal series-pass transistor can still become a problem at the higher currents. We now show some methods of reducing the dissipation.

### 1.2.5 Linear Regulators with PNP Series-Pass Transistors for Reduced Dissipation

Linear regulators using PNP transistors as the series-pass element can operate with a minimum headroom down to less than 0.5 V. Hence they can achieve better efficiency. Typical arrangements are shown in Figure 1.3.

With an NPN series-pass element configured as shown in Figure 1.3a, the base current ( $I_b$ ) must come from some point at a potential higher than  $V_o + V_{be}$ , typically  $V_o + 1$  volts. If the base drive comes through a resistor as shown, the input end of that resistor must come from a voltage even higher than  $V_o + 1$ . The typical choice is to supply the base current from the raw DC input as shown.

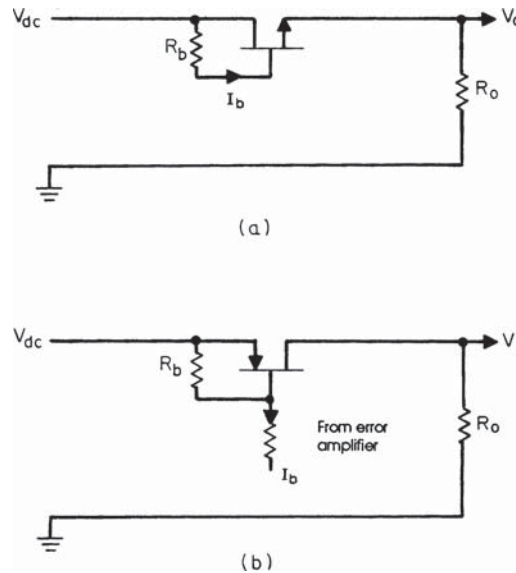
A conflict now exists because the raw DC input at the bottom of the ripple waveform at the low end of the input range cannot be permitted to come too close to the required minimum base input voltage (say,  $V_o + 1$ ). Further, the base resistor  $R_b$  would need to have a very low value to provide sufficient base current at the maximum output current. Under these conditions, at the high end of the input range (when  $V_{dc} - V_o$  is much greater),  $R_b$  would deliver an excessive drive current; a significant amount would have to be diverted away into the current amplifier, adding to its dissipation. Hence a compromise is required. This is why the minimum header voltage is selected to be typically 2.5 V in this arrangement. It maintains a more constant current through  $R_b$  over the range of input voltage.

However, with a PNP series-pass transistor (as in Figure 1.3b), this problem does not exist. The drive current is derived from the common negative line via the current amplifier. The minimum header voltage is defined only by the knee of the  $I_c$  versus  $V_{ce}$  characteristic of the pass transistor. This may be less than 0.5 V, providing higher efficiency particularly for low-voltage, high-current applications.

Although integrated-circuit linear regulators with PNP pass transistors are now available, they are intrinsically more expensive because the fabrication is more difficult.



## 10 Switching Power Supply Design



**FIGURE 1.3** (a) A linear regulator with an NPN series-pass transistor. In this example, the base drive is taken from  $V_{dc}$  via a resistor  $R_b$ . A typical minimum voltage of 1.5 V is required across  $R_b$  to supply the base current, which when added to the base-emitter drop makes a minimum header voltage of 2.5 V. (b) Linear regulator with a PNP series-pass transistor. In this case the base drive ( $I_b$ ) is derived from the negative common line via the drive circuit. The header voltage is no longer restricted to a minimum of 2.5 V, and much lower values are possible.

Similar results can be obtained with NPN transistors by fitting the transistor in the negative return line. This requires the positive line to be the common line. (Normally this would not be a problem in single output supply.)

This completes our overview of linear regulators and serves to demonstrate some of the reasons for moving to the more complicated switching methods for modern, low-weight, small, and efficient power systems.

## 1.3 Switching Regulator Topologies

### 1.3.1 The Buck Switching Regulator

The high dissipation across the series-pass transistor in a linear regulator and the large 60-Hz transformer required for line operation made linear regulators unattractive for modern electronic applications.

Further, the high power loss in the series device requires a large heat sink and large storage capacitors and makes the linear power supply disproportionately large.

As electronics advanced, integrated circuits made the electronic systems smaller. Typically, linear regulators could achieve output power densities of 0.2 to 0.3 W/in<sup>3</sup>, and this was not good enough for the ever smaller modern electronic systems. Further, linear power supplies could not provide the extended hold-up time required for the controlled shutdown of digital storage systems.

Although the technology was previously well known, switching regulators started being widely used as alternatives to linear regulators only in the early 1960s when suitable semiconductors with reasonable performance and cost became available. Typically these new switching supplies used a transistor switch to generate a square-waveform from a non-regulated DC input voltage. This square wave, with adjustable duty cycle, was applied to a low pass output power filter so as to provide a regulated DC output.

Usually the filter would be an inductor (or more correctly a choke, since it had to support some DC) and an output capacitor. By varying the duty cycle, the average DC voltage developed across the output capacitor could be controlled. The low pass filter ensured that the DC output voltage would be the average value of the rectangular voltage pulses (of adjustable duty cycle) as applied to the input of the low pass filter. A typical topology and waveforms are shown later in Figure 1.4.

With appropriately chosen low pass inductor/capacitor (LC) filters, the square-wave modulation could be effectively minimized, and near-ripple-free DC output voltages, equal to the average value of the duty-cycle-modulated raw DC input, could be provided. By sensing the DC output voltage and controlling the switch duty cycle in a negative-feedback loop, the DC output could be regulated against input line voltage changes and output load changes.

Modern very high frequency switching supplies are currently achieving up to 20 W/in<sup>3</sup> compared with 0.3 W/in<sup>3</sup> for the older linear power supplies. Further, they are capable of generating a multiplicity of isolated output voltages from a single input. They do not require a 50/60-Hz isolation power transformer, and they have efficiencies from 70% up to 95%. Some DC/DC converter designers are claiming load power densities of up to 50 W/in<sup>3</sup> for the actual switching elements.

### 1.3.1.1 Basic Elements and Waveforms of a Typical Buck Regulator

**After Pressman** *In the interest of simplicity, Mr. Pressman describes fixed-frequency operation for the following switching regulator examples. In such regulators the on period of the power device ( $T_{on}$ ) is adjusted to maintain*

## 12 Switching Power Supply Design

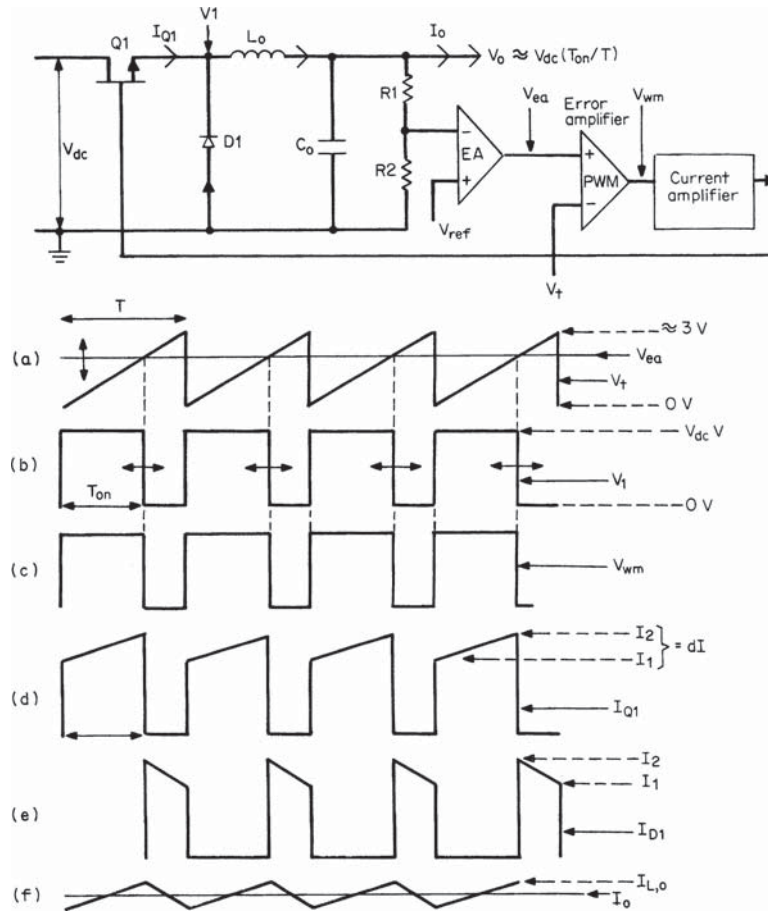


FIGURE 1.4 Buck switching regulator and typical waveforms.

regulation, while the total cycle period ( $T$ ) is fixed, and the frequency is thus fixed at  $1/T$ .

The ratio  $T_{on}/T$  is normally referred to as the duty ratio or duty cycle ( $D$ ) in many modern treatises. In other books on the subject, you may find this shown as  $T_{on}/(T_{on} + T_{off})$ , where  $T_{off}$  is the off period of the power device so that  $T_{on} + T_{off} = T$ . Operators  $D$  and  $M$  are also used in various combinations but essentially refer to the same quantity.

Bear in mind that other modes of operation can be and are used. For example, the on period can be fixed and the frequency changed, or a combination of both may be employed.

The terms  $dI$ ,  $di$ ,  $dV$ ,  $dv$ ,  $dT$  and  $dt$  are used somewhat loosely in this book and normally refer to the changes  $\Delta I$ ,  $\Delta V$ , and  $\Delta t$ , where, for example, in the

*limit,  $\Delta I/\Delta t$  goes to the derivative  $di/dt$ , giving the rate of change of current with time or the slope of the waveform. Since in most cases the waveform slopes are linear the result is the same so this becomes a moot point. ~K.B.*

### 1.3.1.2 Buck Regulator Basic Operation

The basic elements of the buck regulator are shown in Figure 1.4. Transistor  $Q1$  is switched hard “on” and hard “off” in series with the DC input  $V_{dc}$  to produce a rectangular voltage at point  $V1$ . For fixed-frequency duty-cycle control,  $Q1$  conducts for a time  $T_{on}$  (a small part of the total switching period  $T$ ). When  $Q1$  is “on,” the voltage at  $V1$  is  $V_{dc}$ , assuming for the moment the “on” voltage drop across  $Q1$  is zero.

A current builds up in the series inductor  $L_o$  flowing toward the output. When  $Q1$  turns “off,” the voltage at  $V1$  is driven rapidly toward ground by the current flowing in inductor  $L_o$  and will go negative until it is caught and clamped at about  $-0.8$  V by diode  $D1$  (the so-called free-wheeling diode).

Assume for the moment that the “on” drop of diode  $D1$  is zero. The square voltage shown in Figure 1.4b would be rectangular, ranging between  $V_{dc}$  and ground, (0 V) with a “high” period of  $T_{on}$ . The average value of this rectangular waveform is  $V_{dc}T_{on}/T$ . The low pass  $L_oC_o$  filter in series between  $V1$  and the output  $V$  extracts the DC component and yields a clean, near-ripple-free DC voltage at the output with a magnitude  $V_o$  of  $V_{dc}T_{on}/T$ .

To control the voltage,  $V_o$  is sensed by sampling resistors  $R1$  and  $R2$  and compared with a reference voltage  $V_{ref}$  in the error amplifier (EA). The amplified DC error voltage  $V_{ea}$  is fed to a pulse-width-modulator (PWM). In this example the PWM is essentially a voltage comparator with a sawtooth waveform as the other input (see Figure 1.4a). This sawtooth waveform has a period  $T$  and amplitude typically in the order of 3 V. The high-gain PWM voltage comparator generates a rectangular output waveform ( $V_{wm}$ , see Figure 1.4c) that goes high at the start of the sawtooth ramp, and goes low the instant the ramp voltage crosses the DC voltage level from the error-amplifier output. The PWM output pulse width ( $T_{on}$ ) is thus controlled by the EA amplifier output voltage.

The PWM output pulse is fed to a driver circuit and used to control the “on” time of transistor switch  $Q1$  inside the negative-feedback loop. The phasing is such that if  $V_{dc}$  goes slightly higher, the EA DC level goes closer to the bottom of the ramp, the ramp crosses the EA output level earlier, and the  $Q1$  “on” time decreases, maintaining the output voltage constant. Similarly, if  $V_{dc}$  is reduced, the “on” time of  $Q1$  increases to maintain  $V_o$  constant. In general, for all changes, the “on” time of  $Q1$  is controlled so as to make the sampled DC output voltage  $V_o R_2/(R_1 + R_2)$  closely track the reference voltage  $V_{ref}$ .

## 14 Switching Power Supply Design

### 1.3.2 Typical Waveforms in the Buck Regulator

In general, the major advantage of the switching regulator technique over its linear counterpart is the elimination of the power loss intrinsic in the linear regulator pass element.

In the switching regulator the pass element is either fully “on” (with very little power loss) or fully “off” (with negligible power loss). The buck regulator is a good example of this—it has low internal losses and hence high power conversion efficiency.

However, to fully appreciate the subtleties of its operation, it is necessary to understand the waveforms and the magnitude and timing of the currents and voltages throughout the circuit. To this end we will look in more detail at a full cycle of events starting when  $Q1$  turns fully “on.” For convenience we will assume ideal components and steady-state conditions, with the amplitude of the input voltage  $V_{dc}$  constant, exceeding the output voltage  $V_o$ , which is also constant.

When  $Q1$  turns fully “on,” the supply voltage  $V_{dc}$  will appear across the diode  $D1$  at point  $V1$ . Since the output voltage  $V_o$  is less than  $V_{dc}$ , the inductor  $L_o$  will have a voltage impressed across it of  $(V_{dc} - V_o)$ . With a constant voltage across the inductor, its current rises linearly at a rate given by  $di/dt = (V_{dc} - V_o)/L_o$ . (This is shown in Figure 1.4d as a ramp that sits on top of the step current waveform.)

When  $Q1$  turns “off,” the voltage at point  $V1$  is driven toward zero because it is not possible to change the previously established inductor current instantaneously. Hence the voltage polarity across  $L_o$  immediately reverses, trying to maintain the previous current. (This polarity reversal is often referred to as the *flyback* or *inductive kickback* effect of the inductor.) Without diode  $D1$ ,  $V1$  would have gone very far negative, but with  $D1$  fitted as shown, as the  $V1$  voltage passes through zero,  $D1$  conducts and clamps the left side of  $L_o$  at one diode drop below ground. The voltage across the inductor has now reversed, and the current in the inductor and  $D1$  will ramp down, returning to its original starting value, during the “off” period of  $Q1$ .

More precisely, when  $Q1$  turns “off,” the current  $I_2$  (which had been flowing in  $Q1$ ,  $L_o$  and the output capacitor  $C_o$  and the load just prior to turning “off”) is diverted and now flows through diode  $D1$ ,  $L_o$  and the output capacitor and load, as shown in Figure 1.4e. The voltage polarity across  $L_o$  has reversed with a magnitude of  $(V_o + 1)$ . The current in  $L_o$  now ramps down linearly at a rate defined by the equation  $di/dt = (V_o + 1)/L_o$ . This is the downward ramp that sits on a step in Figure 1.4e. Under steady-state conditions, at the end of the  $Q1$  “off” time, the current in  $L_o$  will have fallen to  $I_1$  and is still flowing through  $D1$ ,  $L_o$  and the output capacitor and load.

**Note** Notice the input current is discontinuous with a pulse-like characteristic, whereas the output current remains nearly continuous with some relatively small ripple component depending on the value of  $L_o$  and  $C_o$ . ~ K.B.

Now when  $Q1$  turns “on” again, it initially supplies current into the cathode of  $D1$ , displacing its previous forward current. While the current in  $Q1$  rises toward the previous value of  $I_1$ , the forward  $D1$  current will be displaced, and  $V_1$  rises to near  $V_{dc}$ , back-biasing  $D1$ . Because  $Q1$  is switched “on” hard, this recovery process is very rapid, typically less than  $1\ \mu\text{s}$ .

Notice that the current in  $L_o$  is the sum of the  $Q1$  current when it is “on” (see Figure 1.4d) plus the  $D1$  current when  $Q1$  is “off.” This is shown in Figure 1.4f as  $IL_o$ . It has a DC component and a triangular waveform ripple component  $(I_2 - I_1)$  centered on the mean DC output current  $I_o$ . Thus the value of the current at the center of the ramp in Figure 1.4d and 1.4e is simply the DC mean output current  $I_o$ . As the load resistance and hence load current is changed, the center of the ramp (the mean value) in either Figure 1.4d or 1.4e moves, but the slopes of the ramps remain constant, because during the  $Q1$  “on” time, the ramp rate in  $L_o$  remains the same at  $(V_{dc} - V_o)/L_o$ , and during the  $Q1$  “off” time, it remains the same at  $(V_o + 1)/L$  as the load current changes, because the input and output voltages remain constant.

Because the p-p ripple current remains constant regardless of the mean output current, it will be seen shortly that when the DC current  $I_o$  is reduced to the point where the lower value of the ripple current in Figure 1.4d and 1.4e just reaches zero (the critical load current), there will be a drastic change in performance. (This will be discussed in more detail later.)

### 1.3.3 Buck Regulator Efficiency

To get a general feel for the intrinsic power loss in the buck regulator compared with a linear regulator, we will start by assuming ideal components for transistor  $Q1$  and diode  $D1$  in both topologies. Using the currents shown in Figure 1.4d and 1.4e, the typical conduction losses in  $Q1$  and free-wheeling diode  $D1$  can be calculated and the efficiency obtained. Notice that when  $Q1$  is “off,” it operates at a maximum voltage of  $V_{dc}$  but at zero current. When  $Q1$  is “on,” current flows, but the voltage across  $Q1$  is zero. At the same time,  $D1$  is reverse-biased at a voltage of  $V_{dc}$  but has zero current. (Clearly, if  $Q1$  and  $D1$  were ideal components, the currents would flow through  $Q1$  and  $D1$  with zero voltage drop, and the loss would be zero.)

Hence unlike the linear regulator, which has an intrinsic loss even with ideal components, the intrinsic loss in a switching regulator with

## 16 Switching Power Supply Design

ideal components is zero, and the efficiency is 100%. Thus in the buck regulator, the real efficiency depends on the actual performance of the components. Since improvements are continually being made in semiconductors, we will see ever higher efficiencies.

To consider more realistic components, the losses in the buck circuit are the conduction losses in  $Q1$  and  $D1$  and the resistive winding loss in the choke. The conduction losses, being related to the mean DC currents, are relatively easy to calculate. To this we must add the AC switching losses in  $Q1$  and  $D1$ , and the AC induced core loss in the inductor, so the switching loss is more difficult to establish.

The switching loss in  $Q1$  during the turn “on” and turn “off” transitions is a result of the momentary overlap of current and voltage during the switching transitions. Diode  $D1$  also has switching loss associated with the reverse recovery action of the diode, where again there is a condition of voltage and current stress during the transitions. The ripple waveform in the inductor  $L_o$  results in hysteresis and eddy current loss in the core material. We will now calculate some typical losses.

### 1.3.3.1 Calculating Conduction Loss and Conduction-Related Efficiency

By neglecting second-order effects and AC switching losses, the conduction loss can be quite easily calculated. It can be seen from Figure 1.4d and 1.4e that the average currents in  $Q1$  and  $D1$  during their conduction times of  $T_{on}$  and  $T_{off}$  are the values at the center of the ramps or  $I_o$ , the mean DC output current. These currents flow at a forward voltage of about 1 V over a wide range of currents. Thus conduction losses will be approximately

$$P_{dc} = L(Q1) + L(D1) = 1I_o \frac{T_{on}}{T} + 1I_o \frac{T_{off}}{T} = 1I_o$$

Therefore, by neglecting AC switching losses, the conduction-related efficiency would be

$$\text{Conduction Efficiency} = \frac{P_o}{P_o + \text{losses}} = \frac{V_o I_o}{V_o I_o + 1I_o} = \frac{V_o}{V_o + 1} \quad (1.3)$$

### 1.3.4 Buck Regulator Efficiency Including AC Switching Losses

**After Pressman** *The switching loss is much more difficult to establish, because it depends on many variables relating to the performance of the semiconductors and to the methods of driving the switching devices. Other variables, related to the actual power circuit designs, include the action of any*



snubbers, load line shaping, and energy recovery arrangements. It depends on what the designer may choose to use in a particular design. (See Chapter 11.)

Unless all these things are considered, any calculations are at best only a very rough approximation and can be far from the real values found in the actual design, particularly at high frequencies with the very fast switching devices now available.

**After Pressman** I leave Mr. Pressman's original calculations, shown next, untouched except for some minor editing, because they serve to illustrate the root cause of the switching loss. However, I would recommend that the reader consider using more practical methods to establish the real loss. Many semiconductor manufacturers now provide switching loss equations for their switching devices when recommended drive conditions are used, particularly the modern fast IGBTs (Insulated Gate Bipolar Transistors). Some fast digital oscilloscopes claim that they will actually measure switching loss, providing the real-time device current and voltage is accurately provided to the oscilloscope. (Doing this can also be problematical at very high frequency.)

The method I prefer, which is unquestionably accurate, is to measure the temperature rise of the device in question in a working model. The model must include all the intended snubbers and load line shaping circuits, etc. Replacing the AC current in the device with a DC current to obtain the same temperature rise will provide a direct indication of power loss by simple DC power measurements. This method also allows easy optimization of the drive and load line shaping, which can be dynamically adjusted during operation for minimum temperature rise and hence minimum switching loss. ~ K.B.

Mr. Pressman continues as follows:

Alternating-current switching loss (or voltage/current overlap loss) calculation depends on the shape and timing of the rising and falling voltage and current waveforms. An idealized linear example—which is unlikely to exist in practice—is shown in Figure 1.5a and serves to illustrate the principle.

Figure 1.5a shows the best-case scenario. At the turn “on” of the switching device, the voltage and current start changing simultaneously and reach their final values simultaneously. The current waveform goes from 0 to  $I_o$ , and voltage across Q1 goes from a maximum of  $V_{dc}$  down to zero. The average power during this switching transition is  $P(T_{on}) = \int_0^{T_{on}} IV dt = I_o V_{dc}/6$ , and the power averaged over one complete period is  $(I_o V_{dc}/6)(T_{on}/T)$ .

Assuming the same scenario of simultaneous starting and ending points for the current fall and voltage rise waveforms at the turn “off” transition, the voltage/current overlap dissipation at this transition is given by  $P(T_{off}) = \int_0^{T_{off}} IV dt = I_o V_{dc}/6$  and this power averaged over one complete cycle is  $(I_o V_{dc}/6)(T_{off}/T)$ .



## 18 Switching Power Supply Design

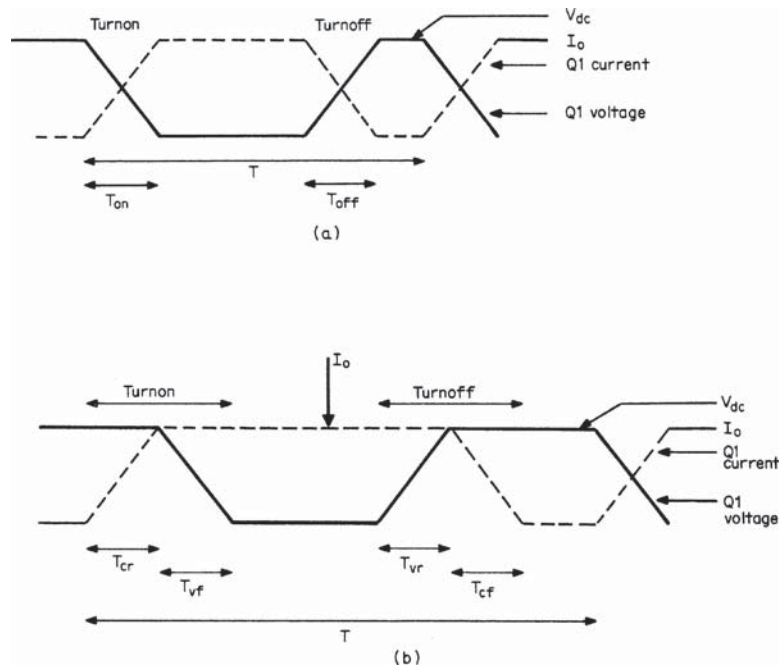


FIGURE 1.5 Idealized transistor switching waveforms. (a) Waveforms show the voltage and current transitions starting and ending simultaneously. (b) Waveforms show the worst-case scenario, where at turn “on” voltage remains constant at  $V_{dc(max)}$  until current reaches its maximum. At turn “off,” the current remains constant at  $I_o$  until Q1 voltage reaches its maximum of  $V_{dc}$ .

Assuming  $T_{on} = T_{off} = T_s$ , the total switching losses (the sum of turn “off” and turn “on” losses) are  $P_{ac} = (V_{dc} I_o T_s)/3T$ , and efficiency is calculated as shown next in Eq. 1.4.

$$\begin{aligned}
 \text{Efficiency} &= \frac{P_o}{P_o + \text{DC losses} + \text{AC losses}} \\
 &= \frac{V_o I_o}{V_o I_o + I_o + V_{dc} I_o T_s / 3T} \\
 &= \frac{V_o}{V_o + 1 + V_{dc} T_s / 3T}
 \end{aligned} \tag{1.4}$$

It would make an interesting comparison to calculate the efficiency of the buck regulator and compare it with that of a linear regulator. Assume the buck regulator provides 5 V from a 48-V DC input at 50-kHz switching frequency ( $T = 20 \mu s$ ).

If there were no AC switching losses and a switching transition period  $T_s$  of  $0.3 \mu\text{s}$  were assumed, Eq. 1.3 would give a conduction loss efficiency of

$$\text{Efficiency} = \frac{5}{5+1} = 83.3\%$$

If switching losses for the best-case scenario as shown in Figure 1.5a were assumed, for  $T_s = 0.3 \mu\text{s}$  and  $T = 20 \mu\text{s}$ , Eq. 1.4 would give a switching-related efficiency of

$$\begin{aligned} \text{Efficiency} &= \frac{5}{5+1+48 \times 0.3/3 \times 20} \\ &= \frac{5}{5+1+0.24} = \frac{5}{5+1.24} \\ &= 80.1\% \end{aligned}$$

If a worst-case scenario were assumed (which is closer to reality), as shown in Figure 1.5b, efficiencies would lower. In Figure 1.5b it is assumed that at turn “on” the voltage across the transistor remains at its maximum value ( $V_{dc}$ ) until the on-turning current reaches its maximum value of  $I_o$ . Then the voltage starts falling. To a close approximation, the current rise time  $T_{cr}$  will equal voltage fall time. Then the turn “on” switching losses will be

$$P(T_{on}) = \frac{V_{dc} I_o}{2} \frac{T_{cr}}{T} + \frac{I_o V_{dc}}{2} \frac{T_{vf}}{T}$$

also for  $T_{cr} = T_{vf} = T_s$ ,  $P(T_{on}) = V_{dc} I_o (T_s / T)$ .

At turn “off” (as seen in Figure 1.5b), we may assume that current hangs on at this maximum value  $I_o$  until the voltage has risen to its maximum value of  $V_{dc}$  in a time  $T_{vr}$ . Then current starts falling and reaches zero in a time  $T_{cf}$ . The total turn “off” dissipation will be

$$P(T_{off}) = \frac{I_o V_{dc}}{2} \frac{T_{vr}}{T} + \frac{V_{dc} I_o}{2} \frac{T_{cf}}{T}$$

With  $T_{vr} = T_{cf} = T_s$ ,  $P(T_{off}) = V_{dc} I_o (T_s / T)$ . The total AC losses (the sum of the turn “on” plus the turn “off” losses) will be

$$P_{ac} = 2V_{dc} I_o \frac{T_s}{T} \quad (1.5)$$

and the total losses (the sum of DC plus AC losses) will be

$$P_t = P_{dc} + P_{ac} = 1I_o + 2V_{dc} I_o \frac{T_s}{T} \quad (1.6)$$

## 20 Switching Power Supply Design

and the efficiency will be

$$\begin{aligned}\text{Efficiency} &= \frac{P_o}{P_o + P_t} = \frac{V_o I_o}{V_o I_o + 1I_o + 2V_{dc}I_o T_s/T} \\ &= \frac{V_o}{V_o + 1 + 2V_{dc}T_s/T}\end{aligned}\quad (1.7)$$

Hence in the worst-case scenario, for the same buck regulator with  $T_s = 0.3 \mu\text{s}$ , the efficiency from Eq. 1.7 will be

$$\begin{aligned}\text{Efficiency} &= \frac{5}{5 + 1 + 2 \times 48 \times 0.3/20} = \frac{5}{5 + 1 + 1.44} \\ &= \frac{5}{5 + 1 + 2.44} \\ &= 67.2\%\end{aligned}$$

Comparing this with a linear regulator doing the same job (bringing 48 V down to 5 V), its efficiency (from Eq. 1.1) would be  $V_o/V_{dc(\text{max})}$ , or 5/48; this is only 10.4% and is clearly unacceptable.

### 1.3.5 Selecting the Optimum Switching Frequency

We have seen that the output voltage of the buck regulator is given by the equation  $V_o = V_{dc}T_{on}/T$ . We must now decide on a value for this period and hence the operating frequency.

The initial reaction may be to minimize the size of the filter components  $L_o, C_o$  by using as high a frequency as possible. However, using higher frequencies does not necessarily minimize the overall size of the regulator when all factors are considered.

We can see this better by examining the expression for the AC losses shown in Eq. 1.5,  $P_{ac} = 2V_{dc}I_o \frac{T_s}{T}$ . We see that the AC losses are inversely proportional to the switching period  $T$ . Further, this equation only shows the losses in the switching transistor; it neglects losses in the free-wheeling diode  $D1$  due to its finite *reverse recovery time* (the time required for the diode to cease conducting reverse current, measured from the instant it has been subjected to a reverse bias voltage). The free-wheeling diode can dissipate significant power and should be of the ultrafast soft recovery type with minimum recovered charge. The reverse recovery time will typically be 35 ns or less.

In simple terms, the more switching transitions there are in a particular period, the more switching loss there will be. As a result there is a trade-off—decreasing the switching period  $T$  (increasing the switching frequency) may well decrease the size of the filter elements, but it will also add to the total losses and may require a larger heat sink.

In general, although the overall volume of the buck regulator will be lower at a higher frequency, the increase in the switching loss and the more stringent high-frequency layout and component-selection requirements make the final choice a compromise among all the opposing elements.

**Note** *The picture is constantly changing as better, lower cost, and faster transistors and diodes are developed. My choice at the present stage of the technology is to design below 100 kHz, as this is less demanding on component selection, layout, and transformer/inductor designs. As a result it is probably lower cost. Generally speaking, higher frequencies absorb more development time and require more experience. However, efficient commercial designs are on the market operating well into the MHz range. The final choice is up to the designer, and I hesitate to recommend a limit because technology is constantly changing toward higher frequency operation. ~ K.B.*

### 1.3.6 Design Examples

#### 1.3.6.1 Buck Regulator Output Filter Inductor (Choke) Design

**Note** *The output inductor and capacitor may be considered a low pass filter, and it is normally treated in this way for transfer function and loop compensation calculations.*

*However, at this stage, the reader may prefer to look upon the inductor as a device that tends to maintain the current reasonably constant during the switching action. (That is, it stores energy when the power device is “on” and transfers this energy to the output when the power device is “off.”)*

*I prefer the term choke for the power inductor, because in this application it must support an element of DC current as well as the applied AC voltage stress. It will be shown later (Chapter 7) that the design of pure inductors (with zero DC current component) is quite different from the design of chokes, with their relatively large DC current component.*

*In the following section Mr. Pressman outlines the parameters that control the design and selection of this critical part. ~ K.B.*

The current waveform of the output inductor (choke) is shown in Figure 1.4f, and its characteristic “dual ramp” shape is defined in Section 1.3.2. Notice that the current amplitude at the center of the ramp is the mean value equal to the DC output current  $I_o$ .

We have seen that as the DC output load current decreases, the slope of the ramp remains constant (because the voltage across  $L_o$  remains constant). But as the mean load current decreases, the ripple current waveform moves down toward zero.

At a load current of half the peak-to-peak magnitude of the ramp,  $I_o = (I_2 - I_1)/2$ , the lower point of the ramp just touches zero.

## 22 Switching Power Supply Design

At this point, the current in the inductor is zero and its stored energy is zero. (The inductor is said to have “run dry.”) If the load current is further reduced, there will be a period when the inductor current remains at zero for a longer period and the buck regulator enters into the “discontinuous current” operating mode. This is an important transition because a drastic change occurs in the current and voltage waveforms and in the closed loop transfer function.

This transition to the discontinuous mode can be seen in the real-time oscilloscope picture of Figure 1.6a. This shows the power switch current waveforms for a buck regulator operating at 25 kHz with an input voltage of 20 V and an output of 5 V as the load current is reduced from a nominal current of 5 A down to about 0.2 A.

The top two waveforms have the characteristic ramp-on-a-step waveshape with the step size reducing as the load current is reduced. The current amplitude at the center of the ramp indicates the effective DC output current.

In the third waveform, where  $I_o = 0.95$  A, the step has gone and the front end of the ramp starts at zero current. This is the *critical load current* indicating the start of the discontinuous current mode (or run-dry mode) for the inductor. Notice that in the first three waveforms, the Q1 “on” time is constant, but decreases drastically as the current is further reduced, moving deeper into the discontinuous mode.

In this example, the control loop has been able to maintain the output voltage constant at 5 V throughout the full range of load currents, even after the inductor has gone discontinuous. Hence it would be easy to assume that there is no problem in permitting the inductor to go discontinuous. In fact there are changes in the transfer function (discussed next) that the control loop must be able to accommodate. Further, the transition can become a major problem in the boost-type topologies discussed later.

For the buck regulator, however, the discontinuous mode is not considered a major problem. For load currents above the onset of the discontinuous mode, the DC output voltage is given by  $V_o = V_1 T_{on}/T$ . Notice the load current is not a parameter in this equation, so the voltage remains constant with load current changes without the need to change the duty ratio. (The effective output resistance of the buck regulator is very low in this region.) In practice the “on” time changes slightly as the current changes, because the forward drop across Q1 and the inductor resistance change slightly with current, requiring a small change in  $T_{on}$ .

If the load is further reduced so as to enter discontinuous mode, the transfer function changes drastically and the previous equation for output voltage ( $V_o = V_1 T_{on}/T$ ) no longer applies. This can be seen in the bottom two waveforms of Figure 1.6a. Notice the “on” time of Q1 has decreased and has become a function of the DC output current.

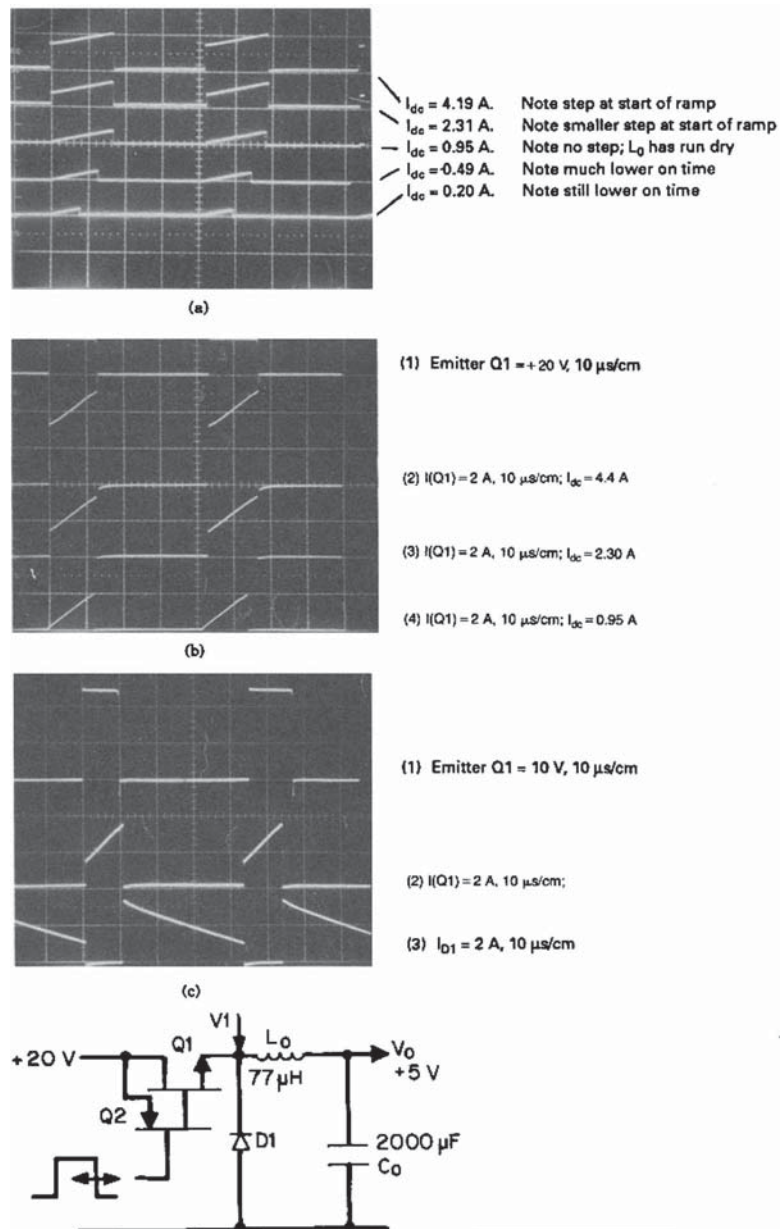


FIGURE 1.6 A 25-kHz buck regulator, showing the transition from the continuous mode to the discontinuous mode at the critical load current, with the inductor  $L_o$  running dry. Note, in Figure 1.6a, line three above, that the “on” time remains constant only so long as the inductor is in the continuous mode.

## 24 Switching Power Supply Design

**TIP** The ratio  $T_{\text{on}}/T$  is normally referred to as the duty ratio  $D$ . The voltage formula for continuous operation is simply  $V_o = V_1 \cdot D$ . However, for discontinuous operation, the duty ratio becomes a function of the load current, and the situation is much more complicated. In the discontinuous mode, the output voltage  $V_o$  is given by the formula

$$V_o = \frac{V_1 \cdot 2D}{D + (D^2 + (8L/RT))^{1/2}}$$

Since the control loop will maintain the output voltage constant, the effective value of the load resistance  $R$  will be inversely proportional to the load current. Hence by holding  $V_o$ ,  $V_1$ ,  $L$ , and  $T$  constant, to maintain the voltage constant, requires that the remaining variable (the duty ratio  $D$ ) must change with load current.

At the critical transition current, the transfer function will change from continuous mode in which the duty ratio remained constant with load change (zero output impedance) to the discontinuous mode in which the duty ratio must change with reducing load current (a finite output impedance). Hence in the discontinuous mode, the control loop must work much harder, and the transient performance will be degraded. ~ K.B.

Dynamically, at load currents above the onset of the discontinuous mode, the output L/C filter automatically accommodated output current changes by changing the amplitude of the step part of the ramp-on-step waveforms shown in the Q1 and D1 waveforms of Figures 1.4d and 1.4e. To the first order, it could do this without changing the Q1 "on" time.

The DC output current is the time average of the Q1 and D1 ramp current. Notice that in Figure 1.6a, line three and line four, that at lower currents where the inductor has gone discontinuous and the step part of the latter waveforms has gone to zero, the only way the current can decrease further is to decrease the Q1 "on" time. The negative-feedback loop automatically adjusts the duty ratio to achieve this.

The dramatic change in the waveforms can be seen very clearly between Figure 1.7a (for the critical current condition) and Figure 1.7b (for the discontinuous condition). Figure 1.7b(2) shows the D1 current going to zero just before Q1 turns "on" (the inductor has dried out and gone discontinuous). With zero current in  $L_o$ , the output voltage will seek to appear at the emitter of Q1. However, the sudden transition results in a decaying voltage "ring," at a frequency determined by  $L_o$  and the distributed capacitance looking into the D1 cathode and Q1 emitter junction at point V1. This is shown in Figure 1.7b(1).

**TIP** Although the voltage ring is not damaging, in the interest of RFI reduction, it should be suppressed by a small R/C snubber across D1. ~ K.B.



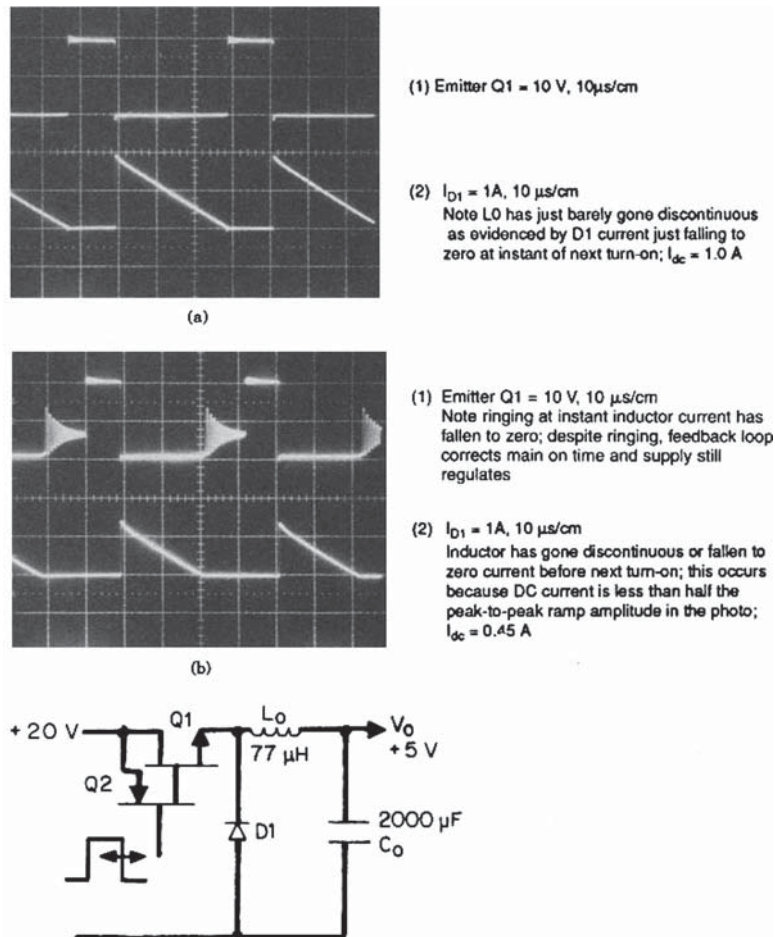


FIGURE 1.7 A 25-kHz buck regulator with typical waveforms. Q1 emitter voltage waveforms and D1 current waveforms for continuous conduction at the critical current (a) and in the discontinuous mode (b).

### 1.3.6.2 Designing the Inductor to Maintain Continuous Mode Operation

Although we have shown that operating in the discontinuous mode is not necessarily a major problem in the buck regulator, it can become a problem in some applications, particularly in boost-type topologies. The designer has the option to design the inductor so that it remains in the continuous mode for the full range of expected (but limited) load currents, as described next.



## 26 Switching Power Supply Design

In this example the inductor will be chosen so that the current remains continuous if the DC output current stays above a specified minimum value. (Typically this is chosen to be around 10% of the rated load current, or  $0.1 I_{\text{on}}$ , where “ $I_{\text{on}}$ ” is defined as the nominal output current.)

The inductor current ramp is  $dI = (I_2 - I_1)$ , as shown in Figure 1.4d. Since the onset of the discontinuous mode occurs at a DC current of half this amplitude, then

$$I_o(\text{min}) = 0.1 I_{\text{on}} = (I_2 - I_1)/2 \quad \text{or} \quad (I_2 - I_1) = dI = 0.2 I_{\text{on}}$$

Also

$$dI = V_L T_{\text{on}}/L = (V_1 - V_o) T_{\text{on}}/L$$

where  $V_1$  is voltage at the input of Q1 and is very close to  $V_{\text{dc}}$ , then

$$L = \frac{(V_{\text{dc}} - V_o) T_{\text{on}}}{dI} = \frac{(V_{\text{dc}} - V_o) T_{\text{on}}}{0.2 I_{\text{on}}}$$

where  $T_{\text{on}} = V_o T / V_{\text{dc}}$  and  $V_{\text{dcn}}$  and  $I_{\text{on}}$  are nominal values, then

$$L = \frac{5(V_{\text{dcn}} - V_o) V_o T}{V_{\text{dcn}} I_{\text{on}}} \quad (1.8)$$

Thus, if  $L$  is selected from Eq. 1.8, then

$$dI = (I_2 - I_1) = 0.2 I_{\text{on}}$$

where  $I_{\text{on}}$  is the center of the inductor current ramp at nominal DC output current.

Since the inductor current will swing  $\pm 10\%$  around its center value  $I_{\text{on}}$ , the inductor must be designed so that it does not significantly saturate at a current of at least  $1.1 I_{\text{on}}$ .

Chapter 7, Section 7.6 provides information for the optimum design of inductors and chokes.

### 1.3.6.3 Inductor (Choke) Design

In the preceding example, continuous mode operation is required, so the current must not reach zero for the full range of load currents. Thus the inductor must support a DC current component and should be designed as a choke.

Well-designed chokes have a low, but relatively constant, inductance under AC voltage stress and DC bias conditions. Typically chokes use either gapped ferrite cores or composite cores of

various powdered ferromagnetic alloys, including powdered iron or Permalloy, a magnetic alloy of nickel and iron. Powdered cores have a distributed air-gap because they are made from a suspension of powdered ferromagnetic particles, embedded in a nonmagnetic carrier to provide a uniformly distributed air-gap. The inductor value calculated by Eq. 1.8 must be designed so that it does not saturate at the specified peak current (110% of  $I_{on}$ ). The design of such chokes is described in more detail in Chapter 7, Section 7.6.

The maximum range of current in the buck regulator will be determined by the choke design, the ratings of the power components, and the DC and AC losses given by Eq. 1.6. To remain in continuous conduction, the minimum current must not go below 10% of the rated  $I_{on}$ . Below this the load regulation will degrade slightly.

This wide (90%) industry standard dynamic load range results in a relatively large choke, which may not be acceptable. However, the designer has considerable flexibility of choice with some trade-offs. If a smaller choke is chosen (say, half the value given by Eq. 1.8), it will go discontinuous at one-fifth rather than one-tenth of the nominal DC output current. This will degrade the load regulation slightly, commencing at the higher minimum current. But since it has less inductance, the buck regulator will respond more quickly to dynamic load changes.

### 1.3.7 Output Capacitor

The output capacitor ( $C_o$ ) shown in Figure 1.4 is chosen to satisfy several requirements.  $C_o$  will not be an ideal capacitor, as shown in Figure 1.8. It will have a parasitic resistance  $R_o$  and inductance  $L_o$  in series with its ideal pure capacitance  $C_o$  as shown. These are referred to as the *equivalent series resistance* (ESR) and *equivalent series inductance* (ESL). In general, if we consider the bulk ripple current amplitude in the series choke  $L_f$ , we would expect the majority of this ripple current to flow into the output capacitor  $C_o$ . Hence the output voltage ripple will be determined by the value of the output filter capacitor,  $C_o$ , its equivalent series resistance (ESR),  $R_o$ , and its equivalent series inductance (ESL),  $L_o$ .

For low-frequency ripple currents,  $L_o$  can be neglected and the output ripple is mainly determined by  $R_o$  and  $C_o$ .

**Note** *The actual transition frequency depends on the design of the capacitor, and manufacturers are constantly improving. Typically it will be above 500 kHz. ~ K.B*

So below about 500 kHz,  $L_o$  can normally be neglected. Typically  $C_o$  is a relatively large electrolytic, so that at the switching frequency,

## 28 Switching Power Supply Design

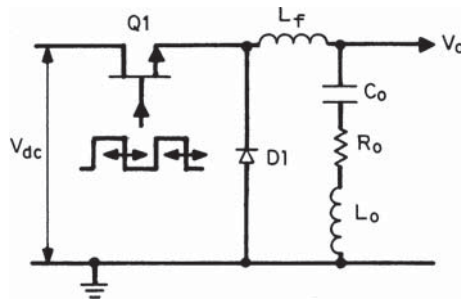


FIGURE 1.8 Output capacitor  $C_o$  showing parasitic components.

the ripple voltage component contributed by  $C_o$  is small compared with that contributed by  $R_o$ . Thus at the mid-frequencies, to the first order, the output ripple is closely given by the AC ripple current in  $L_f$  times  $R_o$ .

More precisely, there are two ripple components due to each of  $R_o$  and  $C_o$ . They are not in phase because that generated by  $R_o$  is proportional to  $I_2 - I_1$  (the peak-to-peak inductor ramp current of Figure 1.4f) and that due to  $C_o$  is proportional to the integral of that current. However, for a worst-case comparison we can assume that they are in phase.

To obtain these ripple voltage components and to permit capacitor selection, it is necessary to know the values of the ESR  $R_o$ , which are seldom given by capacitor manufacturers. An examination of a number of manufacturers' catalogs shows that for the older types (aluminum electrolytic) for a large range of voltage ratings and capacitance values,  $R_o C_o$  tends to be constant. It ranges from  $50$  to  $80 \times 10^{-6} \Omega F$ .

**After Pressman** *Modern low-ESR electrolytic capacitors are now designed for this application, and the ESR values are provided by the manufacturers. If the low-ESR types are chosen, then clearly the lower ESR values should be used in the following calculations. ~ K.B.*

It is instructive to calculate the capacitive and resistive ripple components for a typical buck regulator.

#### Design Example:

Assume a design for a 25-kHz buck regulator with a step down from 20 V to 5 V with a load current  $I_{on} = 5$  A. Let's require the ripple voltage to be below 50 millivolts with continuous conduction down to 10% load.

Assuming the minimum load is to be 10%, then  $I_{o(\min)} = 0.1I_{\text{on}} = 0.5 \text{ A}$ . We will calculate  $L$  from Eq. 1.8:

$$L = \frac{5(V_{\text{dcn}} - V_o)V_o T}{V_{\text{dcn}}I_{\text{on}}} = \frac{5(20 - 5)5 \times 40 \times 10^{-6}}{20 \times 5} = 150 \mu\text{H}$$

Now  $dI$  (the peak-to-peak ramp amplitude) is  $(I_2 - I_1) = 0.2I_{\text{on}} = 1 \text{ A}$ .

If we assume the majority of the output ripple voltage will be produced by the capacitor ESR ( $R_o$ ), we can simply select a capacitor value such that the ESR will satisfy the ripple voltage as follows:

With a resistive ripple component of  $V_{\text{rr}} = 0.05 \text{ V}$  peak-to-peak, then the required ESR  $R_o = V_{\text{rr}}/dI = 0.05/(I_2 - I_1)$  and  $R_o = 0.05 \Omega$ .

Using the preceding typical ESR/capacitance relationship ( $R_o C_o = 50 \times 10^{-6}$ ):

$$C_o = 50 \times 10^{-6}/0.05 = 1000 \mu\text{F}$$

**Note** Clearly, for modern low ESR capacitors, we would use the published ESR values. ~ K.B.

We will now calculate the ripple voltage contribution from the capacitance, ( $C_o = 1000 \mu\text{F}$ ).

Calculating the capacitive ripple voltage  $V_{\text{cr}}$  from Figure 1.4d, it is seen that the ripple current is positive from the center of the “off” time to the center of the “on” time or for one-half of a period, or  $20 \mu\text{s}$  in this example. The average value of this triangle of current is  $(I_2 - I_1)/4 = 0.25 \text{ A}$ . This current produces a ripple voltage across the pure capacitance part  $C_o$  of

$$V_{\text{cr}} = \frac{It}{C_o} = \frac{0.25 \times 20 \times 10^{-6}}{1000 \times 10^{-6}} = 0.005 \text{ V}$$

The ripple current below the  $I_o$  line in Figure 1.4f yields another 0.005-V ripple for a total peak-to-peak capacitive ripple voltage of 0.01 V (only 10 millivolts compared with the resistive component of 50 millivolts). Thus, in this particular case, the ripple due to the capacitance is relatively small compared with that due to the ESR resistor  $R_o$  and to the first order may be ignored.

In the preceding example, the filter capacitor was chosen to yield the desired peak-to-peak ripple voltage by choosing a capacitor with a suitable ESR  $R_o$  from

$$R_o = \frac{V_{\text{or}}}{I_2 - I_1} = \frac{V_{\text{or}}}{0.2I_{\text{on}}} \quad (1.9)$$

### 30 Switching Power Supply Design

Using the typical relationship that the  $R_o C_o$  product will be near  $65 \times 10^{-6}$ :

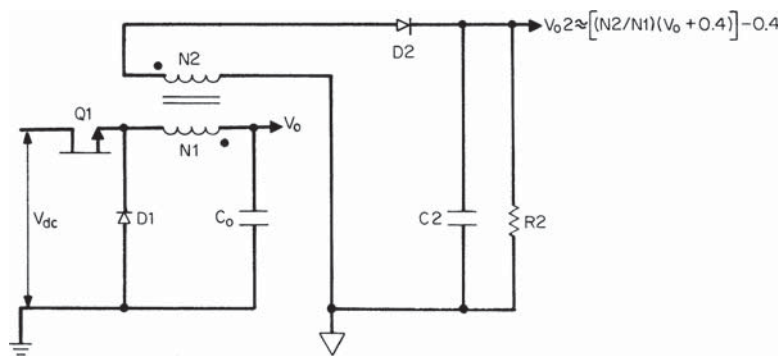
$$C_o = \frac{65 \times 10^{-6}}{R_o} = (65 \times 10^{-6}) \frac{0.2I_{on}}{V_{or}} \quad (1.10)$$

The justification for this approach is demonstrated more generally in the paper by K.V. Kantak.<sup>1</sup> He shows that if  $R_o C_o$  is larger than half the transistor “on” time and half the transistor “off” time—which is the more usual case—the output ripple is determined by the ESR resistor as shown above.

#### 1.3.8 Obtaining Isolated Semi-Regulated Outputs from a Buck Regulator

Very often, low-power ancillary outputs are required for various control functions. This can be done with few additional components as shown in Figure 1.9. The regulation in the additional outputs is typically of the order of 2 to 3%.

It can be seen in Figure 1.4 that the return end of the regulated output voltage is common with the return end of the raw DC input. In Figure 1.9, a second winding with  $N_2$  turns is added to the output filter choke. Its output is peak-rectified with diode  $D_2$  and capacitor  $C_2$ . The start of the  $N_1$ ,  $N_2$  windings is shown by the dots. When  $Q_1$  turns “off,” the finish of  $N_1$  goes negative and is caught at one diode drop below ground by free-wheeling diode  $D_1$ . Since the main output  $V_o$  is regulated against line and load changes, the reverse voltage across



**FIGURE 1.9** Showing how a second isolated output can be derived from a buck regulator by using the output choke as a transformer. The second output is DC-isolated from input ground and is regulated to within about 2 to 3%, as its primary is powered from the regulated  $V_o$  output and the fixed clamped voltage at the cathode of  $D_1$  when  $Q_1$  turns “off.”

$N_1$  is constant as long as the free-wheeling diode  $D_1$  continues to conduct. Using a low-forward-drop Schottky diode for  $D_1$ , its forward drop remains constant at about 0.4 V over a large range of DC output current.

Thus when  $Q_1$  turns “off,” the voltage across  $N_2$  is relatively constant at  $N_2/N_1 (V_o + 0.4)$  volts with its dot end positive. This is peak rectified by  $D_2$  and  $C_2$  to yield  $V_{o2} = N_2/N_1(V_o + 0.4) - 0.4$  if  $D_2$  is also a Schottky diode. This output is independent of the supply voltage  $V_{dc}$  as  $D_2$  is reverse biased when  $Q_1$  turns “on.” Capacitor  $C_2$  should be selected to be large enough that the ancillary voltage does not decay too much during the maximum  $Q_1$  “on” time. Since  $N_2$  and  $N_1$  are isolated from each another, the ancillary output can be isolated or referenced to any other part of the circuit.

**TIP** *This can be a useful technique, but use it with care; notice the ancillary power is effectively stolen from the main output during the reverse recovery of the choke. Hence the main output power needs to be much larger than the total ancillary power to maintain  $D_1$  in conduction. A minimum load will be required on the main output if the ancillary outputs are to be maintained. Notice that using the ancillary outputs to power essential parts of the control circuit can have problems, as the system may not start. ~ K.B.*

## 1.4 The Boost Switching Regulator Topology

### 1.4.1 Basic Operation

The buck regulator topology shown in Figure 1.4 has the limitation that it can only produce a lower voltage from a higher voltage. For this reason it is often referred to as a *step-down* regulator.

The boost regulator (Figure 1.10) shows how a slightly different topology can produce a higher regulated output voltage from a lower unregulated input voltage. Called a *boost regulator* or a *ringing choke*, it works as follows.

An inductor  $L_1$  is placed in series with  $V_{dc}$  and a switching transistor  $Q_1$  to common. The bottom end of  $L_1$  feeds current to  $Q_1$  when  $Q_1$  is “on” or the output capacitor  $C_o$  and load resistor through rectifying diode  $D_1$  when  $Q_1$  is “off.”

Assuming steady-state conditions, with the output voltage and current established, when  $Q_1$  turns “on” (for a period  $T_{on}$ ),  $D_1$  will be reverse biased and does not conduct. Current ramps up linearly in  $L_1$  to a peak value  $I_p = V_{dc}T_{on}/L_1$ .

During the  $Q_1$  “on” time, the output current is supplied entirely from  $C_o$ , which is chosen to be large enough to supply the load current for the time  $T_{on}$  with the specified minimum droop.

## 32 Switching Power Supply Design

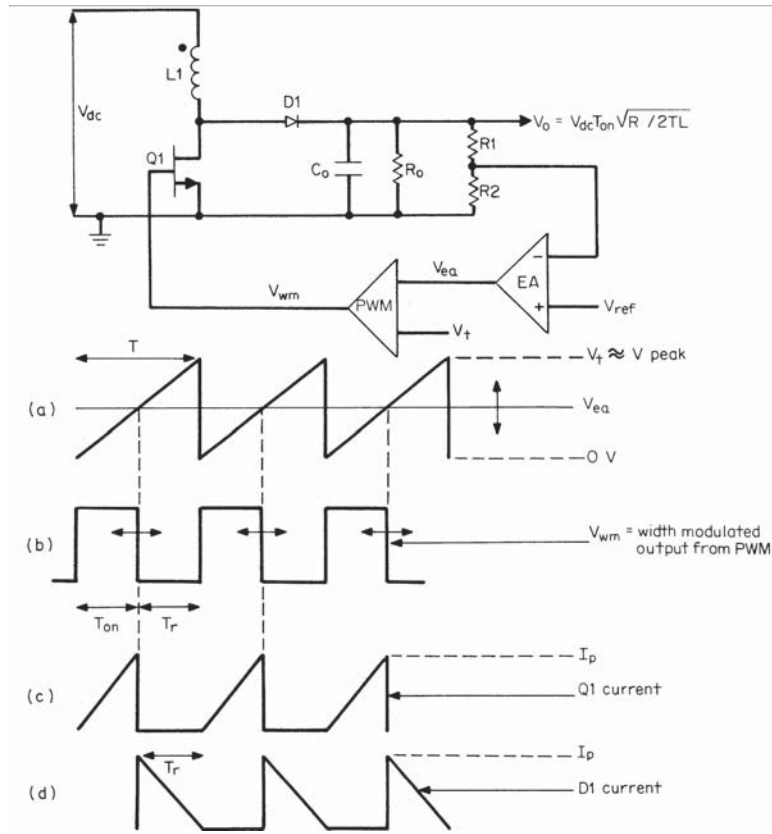


FIGURE 1.10 Boost regulator and critical waveforms. Energy stored in  $L1$  during the  $Q1$  "on" time is delivered to the output via  $D1$  at a higher output voltage when  $Q1$  turns "off" and the polarity across  $L1$  reverses.

When  $Q1$  turns "off," since the current in an inductor cannot change instantaneously, the voltage across  $L1$  reverses in an attempt to maintain the current constant. Now the lower end of  $L1$  goes positive with respect to the input voltage. With the output voltage  $V_o$  higher than the input  $V_{dc}$ ,  $L1$  delivers its stored energy to  $C_o$  via  $D1$ . Hence  $C_o$  is *boosted* to a higher voltage than  $V_{dc}$ . This energy replenishes the charge drained away from  $C_o$  when  $D1$  was not conducting. At the same time current is also supplied to the load from  $V_{dc}$  via  $L1$  and  $D1$  during this action.

In simple terms, the output voltage is regulated by controlling the  $Q1$  "on" time in a negative-feedback loop. If the load current increases,

or the input voltage decreases, the “on” time of Q1 is automatically increased to deliver more energy to the load, or the converse. Hence, in normal operation the “on” period of Q1 is adjusted to maintain the output voltage constant.

### 1.4.2 The Discontinuous Mode Action in the Boost Regulator

**TIP** *The boost regulator has two quite different modes of operation depending on the conduction state of the inductor. If the inductor current reaches zero at the end of a cycle, it is said to operate in a discontinuous mode. If there is some current remaining in the inductor at the end of a cycle, it is said to be in a continuous mode of operation.*

*When speaking about switching regulators, the output filter capacitor is not normally included in the analysis of the converter. The output current of a switching regulator is, therefore, not the DC output current to the load, but rather the combined current that flows in the output capacitor and the load in parallel.*

*Notice that unlike the buck regulator, the boost regulator has a continuous input current (with some ripple current) but a discontinuous output current for all modes of operation. Hence the terms continuous and discontinuous mode refer to what is going on in the inductor.*

*There is a dramatic difference in the transfer function between the two modes of operation that significantly changes the transient performance and intrinsic stability. This is explained more fully in Chapter 12. ~ K.B.*

We will consider in more detail the action for discontinuous mode operation, in which the energy in the inductor is completely transferred to the output during the “off” period of Q1, and we will establish some power and control equations.

We have seen that when Q1 turns “on,” the current ramps up linearly in L1 to a peak value  $I_p = V_{dc}T_{on}/L1$ . Thus energy is stored in L1, and at the end of the “on” period, this stored energy will be

$$E = 0.5L_1I_p^2 \quad (1.11)$$

where  $E$  is in joules,  $L$  is in henries, and  $I_p$  is in amperes.

If the current through D1 (and hence L1) has fallen to zero before the next Q1 turn “on” action, all the energy stored in L1 (Eq. 1.11) during the previous Q1 “on” period will have been delivered to the output load, and the circuit is said to be operating in the discontinuous mode.

The energy  $E$  in joules delivered to the load per cycle, divided by the period  $T$  in seconds, is the output power in watts. Thus if all the energy of Eq. 1.11 is delivered to the load once per period  $T$ , the power



### 34 Switching Power Supply Design

to the load from  $L_1$  alone (assuming for the moment 100% efficiency) would be

$$P_L = \frac{1/2 L (I_p)^2}{T} \quad (1.12)$$

However, during the “off” time of  $Q_1$  ( $T_r$  in Figure 1.10d), the current in  $L_1$  is ramping down toward zero, and the same current is also flowing from the supply  $V_{dc}$  via  $L_1$  and  $D_1$  and is contributing to the load power  $P_{dc}$ . This is equal to the average current during  $T_r$  multiplied by its duty cycle and  $V_{dc}$  as follows:

$$P_{dc} = V_{dc} \frac{I_p}{2} \frac{T_r}{T} \quad (1.13)$$

The total power delivered to the load is then the sum of the two parts as follows:

$$P_t = P_L + P_{dc} = \frac{1/2 L_1 (I_p)^2}{T} + V_{dc} \frac{I_p}{2} \frac{T_r}{T} \quad (1.14)$$

But  $I_p = V_{dc} T_{on} / L_1$ . Substituting for  $I_p$ , in 1.14 we get

$$\begin{aligned} P_t &= \frac{(1/2 L_1) (V_{dc} T_{on} / L_1)^2}{T} + V_{dc} \frac{V_{dc} T_{on}}{2 L_1} \frac{T_r}{T} \\ &= \frac{V_{dc}^2 T_{on}}{2 T L_1} (T_{on} + T_r) \end{aligned} \quad (1.15)$$

To ensure that the current in  $L_1$  has ramped down to zero before the next  $Q_1$  turn “on” action, we set  $(T_{on} + T_r)$  to  $kT$ , where  $k$  is a fraction less than 1. (That is, the period  $T$  is made greater than the inductor conduction period.) Then

$$P_t = (V_{dc}^2 T_{on} / 2 T L_1) (kT)$$

But for an output voltage  $V_o$  and output load resistor  $R_o$ ,

$$P_t = \frac{V_{dc}^2 T_{on}}{2 T L_1} (kT) = \frac{V_o^2}{R_o}$$

or

$$V_o = V_{dc} \sqrt{\frac{k R_o T_{on}}{2 L_1}} \quad (1.16)$$

Thus the negative-feedback loop keeps the output constant against input voltage changes and output load  $R_o$  changes in accordance with Eq. 1.16. As  $V_{dc}$  and  $R_o$  (the load current) go down or up, the loop will increase or decrease  $T_{on}$  so as to keep  $V_o$  constant.

### 1.4.3 The Continuous Mode Action in the Boost Regulator

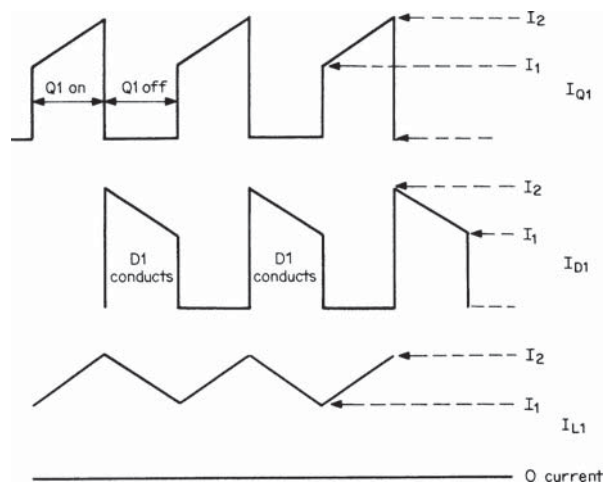
As mentioned in the previous section, if the  $D1$  current (the inductor current) falls to zero before the next turn “on” action, the circuit is said to operate in the discontinuous mode (see Figure 1.10*d*).

However, if the current in  $D1$  and  $L1$  has not fallen to zero at the end of the “on” period, the inductor current will not be zero at the next  $Q1$  turn “on” action. Hence the current in  $Q1$  will have a front-end step as shown in Figure 1.11. The current in the inductor cannot change instantaneously. Currents in  $Q1$  and  $D1$  will have the characteristic ramp-on-a-step waveshape as shown in Figure 1.11.

The circuit is now said to be operating in the continuous mode because the inductor current does not reach zero during a cycle of operation.

Assuming the feedback loop maintains the output voltage constant, as  $R_o$  or  $V_{dc}$  decreases, the feedback loop increases the  $Q1$  “on” period  $T_{on}$  to maintain the output voltage constant. As the load current increases,  $R_o$  or  $V_{dc}$  continues to decrease, a point is reached such that  $T_{on}$  is so large that the decaying current through  $L1$  and  $D1$  will not have fallen to zero before the next turn “on” action, and the action moves into the continuous mode as shown in Figures 1.10 and 1.11.

Now an error-amplifier circuit, which had successfully stabilized the loop while it was operating in the discontinuous mode, may not



**FIGURE 1.11** Typical current waveforms in  $Q1$ ,  $D1$ , and  $L1$  for a boost regulator operating in continuous mode. Note that inductor  $L1$  has not had enough time to transfer all its energy to the load before the next  $Q1$  turn “on” action.

## 36 Switching Power Supply Design

be able to keep the loop stable in the continuous mode and may oscillate. In traditional feedback-loop analysis, the continuous-mode boost regulator has a *right-half-plane-zero in the transfer function*.<sup>2</sup> The only way to stabilize a loop with a right-half-plane-zero is to drastically reduce the error-amplifier bandwidth.

**TIP** *In simple terms, in the discontinuous mode, there is a short period when there is zero current in the inductor and zero current in D1. That is, there is a small time-gap between the energy transfer period (when Q1 is “off” and D1 is conducting) and the energy storage period (when Q1 is “on” and D1 is not conducting). This time margin (dead time) is critical to the way the power system behaves and does not exist in the continuous mode.*

It is very important to fully understand the difference between the two modes of operation, because in any switching topology that has a boost-type behavior, the effect will be evident. To better understand this, we will consider a transient load increase in a continuous mode boost topology and follow the sequence of events as the circuit responds to the load change.

Consider a continuous-mode buck system, running in steady-state conditions, with a stabilized output voltage and a load current that maintains the inductor in continuous conduction. We now apply a sudden increase in load current. The output voltage will tend to fall, and the control loop will increase the “on” period of Q1 to initiate an increase in current in L1. However, it takes several cycles before the current in L1 will increase very much (depending on the value of the inductor, the input voltage, and the actual increase in the Q1 “on” time).

It is important to notice that the immediate effect of increasing the “on” period is to decrease the “off” period (because the total period is fixed). Since D1 only conducts during the “off” period of Q1 (and this period is immediately reduced), the mean output current will initially decrease, rather than increase as was required. Hence we have a situation where we tried to increase the output current, but the immediate effect was to reduce the output current. This will correct itself slowly as the current in the inductor increases over a few cycles.

From a control theory perspective, for a short time this effect introduces an additional 180° of phase shift into the closed loop control system during the transient period when the L1 current is increasing. In terms of control theory this translates to a zero in the right half-plane of the transfer function; it is the cause of the right-half-plane-zero in the small signal transfer function.

Notice that the effect is related to the dynamic behavior of the power components and cannot be changed by the control circuit. In fact, a perfect high-gain fast-response control circuit would result in the “on” period going to the full pulse width on the first pulse, and there would be zero output current for a short period. Hence, the right-half-plane-zero cannot be eliminated by the loop compensation network. The only option is to slow down the rate of change of pulse width to allow the output to keep up without too much droop.

*(In control theory parlance, the control loop must be rolled off at a frequency well below the right-half-plane-zero crossover frequency.)*

*In the discontinuous mode the performance is quite different. The small time-gap margin allows the “on” period to increase without the need to reduce the “off” period (within the limits of the margin), so the problem is not present, providing the margin is large enough to accommodate the change in pulse width.*

*Be aware that in the continuous conduction mode, the right-half-plane-zero effect will be found in any switching converter (or combination of converters and transformers) that has a boost-type action in any part of the circuit. The flyback converter is a typical example of this. The mathematics of this effect will be found in Chapter 12 and reference 2. ~ K.B.*

#### 1.4.4 Designing to Ensure Discontinuous Operation in the Boost Regulator

For the preceding reasons, the designer may prefer to ensure that the boost regulator remains fully within the discontinuous mode for the full range of operating conditions.

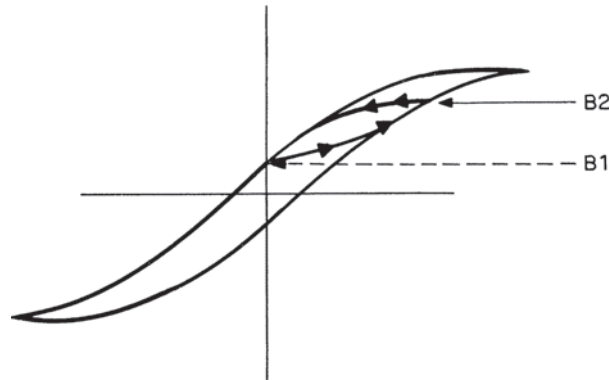
In Figure 1.10d we see that the decaying  $D1$  current just comes down to zero at the start of the next turn “on” action. This is the threshold between discontinuous and continuous mode operation.

This threshold is seen from Eq. 1.16 to occur at certain combinations of  $V_{dc}$ ,  $T_{on}$ ,  $R_o$ ,  $L1$ , and  $T$  that result in the  $L1$ ,  $D1$  current just falling to zero prior to the next turn “on” action of  $Q1$ . It can be seen from Figure 1.10a that any further decrease in  $V_{dc}$  or  $R_o$  (increase in load current) will force the circuit into the continuous mode such that oscillation can occur unless the error amplifier has been rolled off at a very low frequency.

To avoid this problem, we will see from Eq. 1.16 that  $T_{on}$  must be selected so that when it is a maximum (which is when  $V_{dc}$  and  $R_o$  are at their minimum specified values) and the current in  $D1$  has fallen back to zero, there is a usable working dead-time margin ( $T_{dt}$ ) before  $Q1$  turns “on” again.

At the same time, we must ensure that by the time the current in  $D1$  returns to zero, the  $L1$  core will have been restored to its previous starting place on its hysteresis loop, shown as  $B1$  in Figure 1.12. If the core is not fully restored to  $B1$ , then after many such cycles, the starting point will drift up the hysteresis loop and saturate the core. Since the impedance of a saturated core drops to its winding resistance only (because it cannot sustain voltage), the voltage at the transistor collector will suddenly move up to the supply voltage, and with negligible resistance in the path, the transistor will be destroyed.

## 38 Switching Power Supply Design



**FIGURE 1.12** The working B/H loop. A choke core must not be allowed to walk up or down its hysteresis loop. If it is driven from, say, B1 to B2 by a given forward volt-second product, it must be subjected to an equal volt-second product in the opposite direction to restore it to B1 before the next “on” period.

In this example, to ensure that the circuit remains in the discontinuous mode, a dead-time  $T_{dt}$  of 20% of a full period will be provided. Hence we must ensure that the sum of the maximum “on” time of Q1 plus the core reset time plus the dead time will equal a full period, as shown in Figure 1.13. This will ensure that the stored current in L1 will have fallen to zero well before the next Q1 turn “on” action.

Hereafter, a line appearing *below* a term will indicate the *minimum* permitted or specified or required value of that term, and a line appearing *over* a term will indicate the *maximum* value of that term.

Then  $\overline{T_{on}} + T_r + T_{dt} = T$ ,  $\overline{T_{on}} + T_r + 0.2T = T$ ,  
or

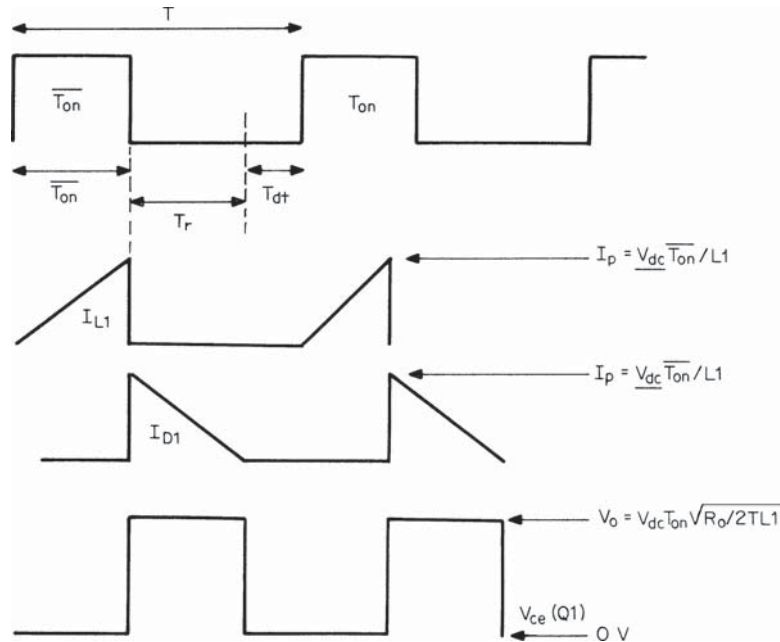
$$\overline{T_{on}} + T_r = 0.8T \quad (1.17)$$

From Eq. 1.16, the maximum “on” time  $\overline{T_{on}}$  occurs at minimum  $\underline{V_{dc}}$  and minimum  $\underline{R_o}$ . Then for the “on” or set volt-second product to equal the “off” or reset volt-second product at minimum  $\underline{R_o}$ :

$$\underline{V_{dc}} \overline{T_{on}} = (V_o - \underline{V_{dc}}) T_r \quad (1.18)$$

Now Eqs. 1.17 and 1.18 have only two unknowns,  $\overline{T_{on}}$  and  $T_r$ , and thus both are determined.  $\overline{T_{on}}$  is then

$$\overline{T_{on}} = \frac{0.8T(V_o - \underline{V_{dc}})}{\underline{V_{dc}}} \quad (1.19)$$



**FIGURE 1.13** Boost regulator waveforms in the discontinuous mode with 20% dead-time margin. For discontinuous-mode operation, the current in  $D1$  (see Figure 1.10) must have decayed to zero before the next turn “on” action. To ensure this, the inductor  $L1$  is chosen such that  $T_{on(max)} + T_r = 0.8T$ , leaving a dead time  $T_{dt}$  of  $0.2T$ .

Now in Eq. 1.16, with  $V_{dc}$  and  $R_o$  (maximum load current) specified,  $T_{on}$  is calculated from Eq. 1.19 and  $k [= (T_{on} + T_r)/T] = 0.8$  from Eq. 1.17.

Inductor  $L1$  is fixed so the circuit is guaranteed not to enter the continuous mode. However, if the output load current is increased beyond its specified maximum value ( $R_o$  decreased below its specified minimum) or  $V_{dc}$  is decreased below its specified minimum, the feedback loop will attempt to increase  $T_{on}$  to keep  $V_o$  constant. This will eat into the dead time,  $T_{dt}$ , and move the circuit closer to continuous mode. To avoid this, we must limit the maximum “on” time or a maximum peak current must be provided.

**TIP** A good method that accounts for all variables is to inhibit the turn “on” of  $Q1$  until the inductor current reaches zero. For fixed-frequency operation this limits the load current. Alternatively it can be set up to provide variable-frequency operation, which is often preferred. ~ K.B.

## 40 Switching Power Supply Design

With  $L_1$  determined earlier from Eq. 1.16,  $V_{dc}$  specified, and  $\overline{T_{on}}$  calculated from Eq. 1.19, the peak current in  $Q_1$  can be calculated from Eq. 1.14, and a transistor selected to have adequate gain at  $I_p$ .

The boost regulator is frequently used at low power levels in non-isolated applications due to the very low parts count. A typical application would be on a printed-circuit board where it is desired to step up a 5-V computer logic level supply to, say, 12 or 15 V for operational amplifiers.

Frequently at higher power levels in battery-supplied power supplies, as the battery discharges, its output voltage drops significantly. Many systems whose prime power is a nominal 12- or 28-V battery will present problems when the battery voltage falls to about 9 or 22 V. Boost regulators are frequently used in such applications to boost the voltages back up to the 12- and 28-V level. Power requirements in such applications can be in the range 50 to 200 watts.

### 1.4.5 The Link Between the Boost Regulator and the Flyback Converter

The boost regulator has been treated in great detail because boost action appears in many converter combinations. For example, by replacing the inductor  $L_1$  with a transformer (more correctly a choke with an additional secondary winding), a very similar, valuable, and widely used topology, the *flyback converter*, is realized.

Like the boost, the flyback stores energy in its magnetics during the “on” period of the power device and transfers the energy to the output load during the “off” period.

Because the secondary windings can be isolated from the input, the outputs are not constrained to share a common return line. Also by using multiple secondaries, a multiple output power supply is possible. The outputs may be higher or lower voltage than the input, and may be common or isolated as required.

The problems of discontinuous or continuous operation and the design relationships and procedures for the flyback are similar to those of the boost regulator and will be discussed in more detail in Chapter 4.

---

## 1.5 The Polarity Inverting Boost Regulator

### 1.5.1 Basic Operation

Figure 1.14 shows a different arrangement of the boost regulator that provides polarity inversion. It uses the same basic principle as the previous boost regulator in that energy is stored in the inductor during the “on” period of  $Q_1$ , which is then transferred to the output load and  $C_o$  in the “off” period of  $Q_1$ .

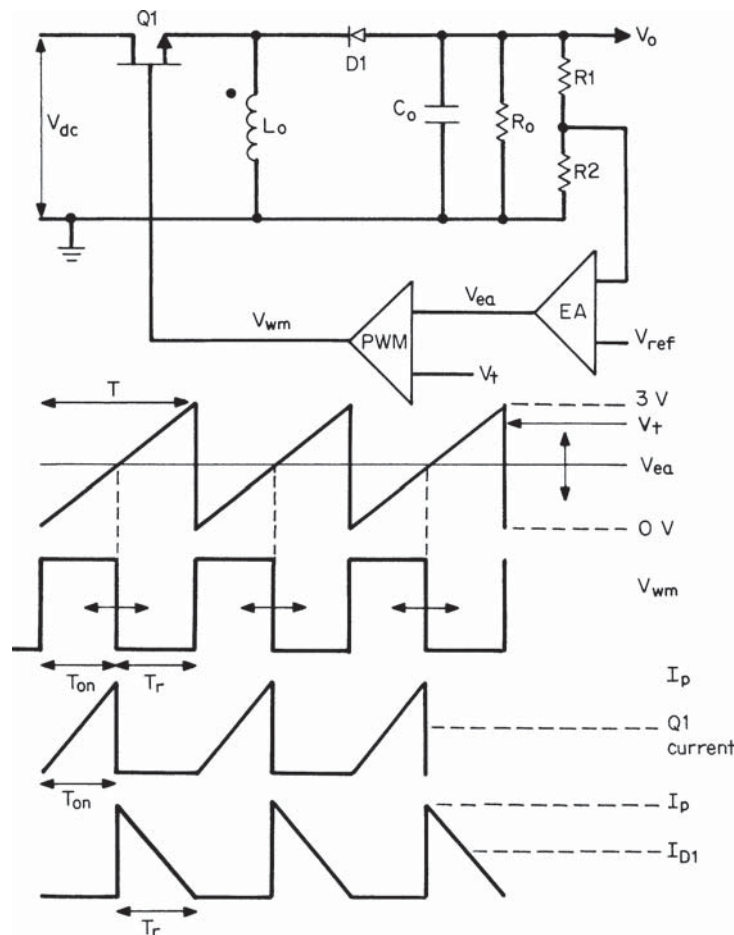


FIGURE 1.14 The polarity-inverting boost regulator and typical waveforms.

Comparing Figures 1.14 and 1.10, it will be seen that the transistor and inductor have changed places. In the reverse polarity inverter, the transistor is above the inductor rather than below it as it was in the boost circuit. Also the rectifying diode has been reversed.

When  $Q1$  turns "on," diode  $D1$  is reverse biased because its cathode is at  $V_{dc}$  (assuming to a close approximation that the voltage drop across  $Q1$  is zero). Also, assuming steady-state conditions, such that  $C_o$  has charged down to some negative voltage, then  $D1$  remains reverse biased throughout the  $Q1$  "on" period. A fixed-voltage  $V_{dc}$  will be impressed across the inductor  $L_o$ , and the current in it ramps up linearly at a rate  $di/dt = V_{dc}/L_o$ .



## 42 Switching Power Supply Design

After an “on” period  $T_{\text{on}}$ , the current in  $L_o$  will have reached  $I_p = V_{\text{dc}}T_{\text{on}}/L_o$ , and the energy stored in  $L_o$  (in joules) is  $E = .5L_o I_p^2$ . When Q1 turns “off,” the voltage polarity across  $L_o$  reverses in an attempt to maintain its current constant. Thus at the instant of turn “off,” the same inductor current  $I_p$  (which was flowing through Q1 before it turned “off”) now continues to flow down through  $L_o$  to common, pulling the current through D1 from  $C_o$ . This current charges the top end of  $C_o$  to a negative voltage.

After a number of cycles, when the required output voltage is developed, the error amplifier adjusts the Q1 “on” period  $T_{\text{on}}$  so that the sampled output voltage  $V_o R_2/(R_1 + R_2)$  is equal to the reference voltage  $V_{\text{ref}}$ . Further, if all the energy stored in  $L_o$  is delivered to the load before the next Q1 turn “on” action (that is,  $I_{D1}$  has fallen to zero), then the circuit operates in the discontinuous mode, and the power delivered to the load will be

$$P_t = \frac{1/2 L_o I_p^2}{T} \quad (1.20)$$

It should be noted that unlike the case of the boost regulator, when Q1 turns “off,” the inductor current does not flow from the supply source (see Eq. 1.13). Hence the only power to the load is that given by Eq. 1.20. Thus assuming 100% efficiency, the output power would be

$$P_o = \frac{V_o^2}{R_o} = \frac{1/2 L_o I_p^2}{T} \quad (1.21)$$

and for  $I_p = V_{\text{dc}}T_{\text{on}}/L_o$ ,

$$V_o = V_{\text{dc}}T_{\text{on}}\sqrt{\frac{R_o}{2TL_o}} \quad (1.22)$$

### 1.5.2 Design Relations in the Polarity Inverting Boost Regulator

As in the previous boost circuit, it is desirable to keep the circuit operating in the discontinuous mode by ensuring that the current stored in  $L_o$  during the Q1 maximum “on” period has decayed to zero at the end of the “off” period  $T_r$ . To ensure this action, we will provide a dead time  $T_{\text{dt}}$  margin of  $0.2T$  before the next Q1 turn “on” action. Thus if  $\overline{T_{\text{on}}} + T_r + T_{\text{dt}} = T$ , then for  $T_{\text{dt}} = 0.2T$  we obtain

$$\overline{T_{\text{on}}} + T_r = 0.8T \quad (1.23)$$

In addition, as in the boost regulator, the “on” volt-second product must equal the reset volt-second product to prevent the core from saturating. Since (as can be seen from Eq. 1.22) the maximum  $\overline{T_{\text{on}}}$  occurs

for minimum  $V_{dc}$  and minimum  $R_o$  (maximum current), it follows that

$$\underline{V_{dc}} T_{on} = V_o T_r \quad (1.24)$$

Thus both Eqs. 1.23 and 1.24 have two unknowns:  $\overline{T_{on}}$  and  $T_r$ . This fixes  $\overline{T_{on}}$  at

$$\overline{T_{on}} = \frac{0.8 V_o T}{\underline{V_{dc}} + V_o} \quad (1.25)$$

Now, with  $\overline{T_{on}}$  calculated from Eq. 1.25 and  $\underline{V_{dc}}$ ,  $\underline{R_o}$ ,  $V_o$ , and  $T$  specified, Eq. 1.22 defines  $L_o$  such that  $I_p = \underline{V_{dc}} \overline{T_{on}} / L_o$ , and transistor Q1 is selected to have adequate gain at  $I_p$ .

---

## References

1. K. V. Kantak, "Output Voltage Ripple in Switching Power Converters," in *Power Electronics Conference Proceedings*, Boxborough, MA, pp. 35–44, April 1987.
2. K. Billings, *Switchmode Power Supply Handbook*, New York: McGraw-Hill, 1999, Chap. 9.

## Basic Topologies

# CHAPTER 2

---

## Push-Pull and Forward Converter Topologies

---

### 2.1 Introduction

In the three switching regulator topologies discussed in the previous chapter, the output returns were all common with the input returns, and multiple outputs were not possible (except for the special case discussed in Section 1.3.8).

In this chapter we look at some of the most widely used fully isolated switching regulator topologies. These topologies—the push-pull, single-ended forward converter, and the double-ended and interleaved forward converters—are similar, so we consider them a single family. All these topologies deliver their power to the loads via a high-frequency transformer; hence outputs may be DC-isolated from the input, and multiple outputs are possible.

---

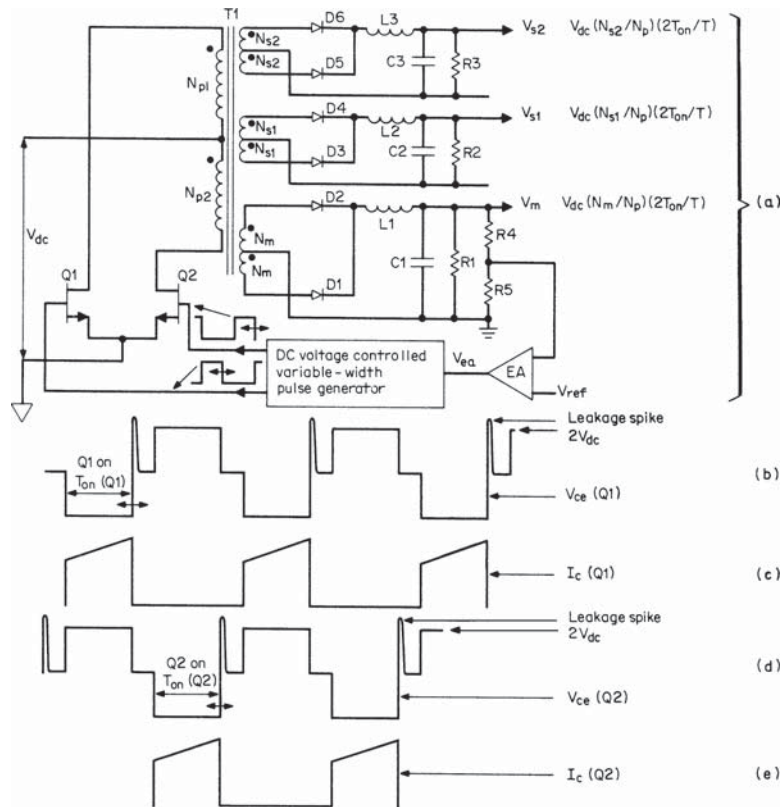
### 2.2 The Push-Pull Topology

#### 2.2.1 Basic Operation (With Master/Slave Outputs)

A push-pull topology is shown in Figure 2.1. It consists of a transformer  $T_1$  with multiple secondaries. Each secondary delivers a pair of  $180^\circ$  out-of-phase square-wave power pulses whose amplitude is fixed by the input voltage and the number of primary and secondary turns.

The pulse widths for all secondaries are identical, as determined by the control circuit and the negative-feedback loop around the *master* output. The control circuit is similar to the buck and boost regulators shown previously in Figures 1.4 and 1.10, except that two equal

## 46 Switching Power Supply Design



**FIGURE 2.1** Push-pull width-modulated converter. Transistors  $Q1$  and  $Q2$  receive 180° out-of-phase, pulse-width modulated drive signals. The master output is  $V_{sm}$ , and there are two slaves,  $V_{s1}$  and  $V_{s2}$ . The feedback loop is closed around  $V_{sm}$ , and the pulse width  $T_{on}$  is controlled to regulate the master output against line and load changes. It will be seen that the slaves are regulated against line changes, but only partially against load changes.

adjustable pulse-width, 180°-out-of-phase pulses drive the bases of  $Q1$ ,  $Q2$ . The additional secondaries  $N_{s1}$ ,  $N_{s2}$  are referred to as *slaves*.

Transistor base drives at turn "on" are sufficient to bring the switched end of each half primary down to  $V_{ce(sat)}$ , typically about 1 V, over the full specified current range. Hence as each transistor turns "on," it applies a square-voltage pulse to its half primary of magnitude  $V_{dc} - 1$ .

On the secondary side of the transformer, there will be flat-topped square waves of amplitude  $(V_{dc} - 1)(N_s/N_p) - V_d$  with a duration  $T_o$ , where  $V_d$  is an output rectifier forward drop, taken as 1 V for a

## Chapter 2: Push-Pull and Forward Converter Topologies 47

conventional fast-recovery diode, and 0.5 V for a Schottky diode. The output pulses at the rectifier cathodes have a duty cycle of  $2T_{\text{on}}/T$  because there are two pulses per period.

Thus the waveforms at the inputs to the  $LC$  filters shown in Figure 2.1 are very much like that at the input to the buck regulator  $LC$  filter of Figure 1.4, which has a flat-topped amplitude and adjustable width. The  $LC$  filters of Figure 2.1 serve the same purpose as that of Figure 1.4. They provide a DC output that is the average of the square wave voltage at the input of the filter. The analysis of the inductor and capacitor functions proceeds exactly as for the buck regulator, and the method of calculating their magnitudes is exactly the same as follows.

The DC or average voltage at the  $V_m$  output in Figure 2.2 (assuming  $D1, D2$  are 0.5-V forward-drop Schottky diodes) will be

$$V_m = \left[ (V_{\text{dc}} - 1) \left( \frac{N_m}{N_p} \right) - 0.5 \right] \frac{2T_{\text{on}}}{T} \quad (2.1)$$

The waveforms at the  $V_m$  output rectifiers are shown in Figure 2.2. If the negative-feedback loop is closed around  $V_m$  as shown in Figure 2.1,  $T_{\text{on}}$  and  $V_m$  will be regulated against DC input voltage and load

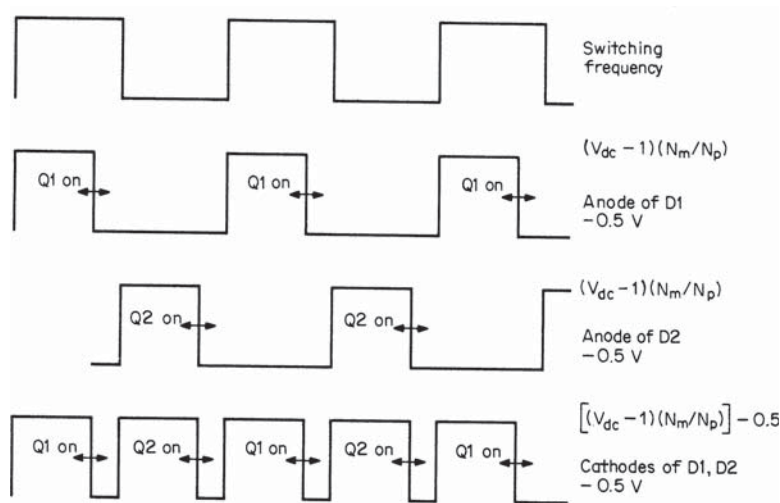


FIGURE 2.2 Voltage waveforms ( $N_m$ ) at the master secondary winding. The output  $LC$  averaging filter yields a DC output voltage.

$$V_m = [(V_{\text{dc}} - 1)(N_m/N_p) - 0.5](2T_{\text{on}}/T)$$

As  $V_{\text{dc}}$  varies, the negative-feedback loop corrects  $T_{\text{on}}$  in the direction to keep  $V_m$  constant.

## 48 Switching Power Supply Design

current changes. Although load current does not appear in Eq. 2.1, a current change will cause  $V_m$  to change, that change will be sensed by the error amplifier, and  $T_{on}$  will be altered to correct it. Providing the current in  $L1$  (see Figure 2.1) does not go discontinuous, changes in  $T_{on}$  will be small, and the absolute value of  $T_{on}$  will be given by Eq. 2.1 for any turns ratio  $N_m/N_p$ , input voltage  $V_{dc}$ , and period  $T$ .

For the slave secondaries, the voltages at the cathodes of the rectifying diodes are fixed by the number of secondary turns, and the  $T_{on}$  duration of the square waves is the same as defined by the master feedback loop. Thus the slave output voltages with normal diodes will be

$$V_{s1} = \left[ (V_{dc} - 1) \frac{N_{s1}}{N_p} - 1 \right] \frac{2T_{on}}{T} \quad (2.2)$$

$$V_{s2} = \left[ (V_{dc} - 1) \frac{N_{s2}}{N_p} - 1 \right] \frac{2T_{on}}{T} \quad (2.3)$$

### 2.2.2 Slave Line-Load Regulation

It can be seen from Eqs. 2.1, 2.2, and 2.3 that the slaves are regulated against  $V_{dc}$  input changes by the negative-feedback loop that keeps  $V_m$  constant, in accordance with Eq. 2.1. The same equation,

$$V_m = (V_{dc} - 1)T_{on}$$

also appears in Eqs. 2.2 and 2.3, and thus  $V_{s1}$ ,  $V_{s2}$  are also kept constant as  $V_{dc}$  changes.

Notice that if load current in the master ( $V_m$ ) changes, the drops across its rectifying diodes and winding resistance will change slightly. Thus the negative-feedback loop will correct for  $V_m$  load change effects and alter  $T_{on}$  to keep  $V_m$  constant.

For the slave outputs,  $T_{on}$  will now change without corresponding changes in  $V_{dc}$ , and from Eqs. 2.2 and 2.3, it can be seen that changes in  $V_{s1}$ ,  $V_{s2}$  will result. Such changes in the slave output voltages due to changes in the master output current are referred to as *cross regulation*.

Slave output voltages will also change as a result of changes in their own output currents. In a similar way slave current changes will cause voltage drop changes in their rectifying diodes and winding resistances, lowering the peak voltages slightly. These changes are not corrected by the main feedback loop, which senses only  $V_m$ .

However, providing the currents in the slave output inductors  $L2$ ,  $L3$ , and especially in the master inductor  $L1$  do not go discontinuous, slave output voltages can be depended on to vary within only  $\pm 5$  to  $\pm 8\%$ .

**TIP** *Much better cross regulation can be obtained by using coupled output inductors (where all outputs share a common inductor core).<sup>1</sup> ~ K.B.*

### 2.2.3 Slave Output Voltage Tolerance

Although changes in slave output voltages are relatively small, the absolute values of output voltage are not accurately adjustable. As seen in Eqs. 2.2 and 2.3, they are fixed by  $T_{on}$  and their corresponding secondary turns  $N_{s1}$ ,  $N_{s2}$ . But  $T_{on}$  is nearly constant, defined by the feedback loop to keep the master voltage constant. Further, since the turns can be changed only by integral numbers, the absolute value of slave output voltage is not finely settable. The change in secondary voltage for a single turn change in  $N_s$  is given by  $V_m \cdot T_{on}/N_p$ .

In most cases, the absolute values of slave output voltage are not too important. Slaves usually drive operational amplifiers or motors, and most often these can tolerate DC voltages within about 2 V of a desired value. If the absolute magnitude is important, the output voltage is usually designed to be higher than required and brought down to a desired exact value with a linear or buck regulator. Because a slave output is semi-regulated, a linear regulator is reasonably efficient.

### 2.2.4 Master Output Inductor Minimum Current Limitations

The selection of the output inductor for a buck regulator was discussed in Section 1.3.6. It was mentioned that at the average current in which the step at the front of the inductor current waveform has fallen to zero (see Figures 1.6a and 1.6b), the inductor is said to run dry or to go discontinuous. Below this average current, the feedback loop maintains the buck regulator's output voltage constant by reducing the "on" period; this results in reduction of slave output voltages.

In Figure 1.6a, however, it can be seen that at currents above going discontinuous, the "on" time is very nearly constant over large output current changes. Below run-dry, the "on" time changes drastically. In the buck regulator this does not pose a major problem because only one output is involved and the feedback loop keeps this output voltage constant. But in the push-pull width-modulated converter with a master and some slaves, the slave output voltages are directly proportional to the master "on" time, as shown by Eqs. 2.2 and 2.3.

Hence, when slaves are involved it is important that the average master output inductor current not be permitted to go discontinuous above its specified minimum. If the master minimum output current is specified at one-tenth its nominal value for example, a minimum output inductor value must be selected from Eq. 1.8. The slave output voltages will vary within about 5% above the master inductor



## 50 Switching Power Supply Design

discontinuous current. Below this critical current, the feedback loop will keep the master output voltage constant by decreasing  $T_{on}$  significantly, followed by the slave output voltages.

Further, the slave outputs must not be permitted to go discontinuous above their own specified minimum currents. Slave output inductors should also be selected from Eq. 1.8. Clearly, larger minimum currents imply smaller inductors.

**TIP** *This problem is also eliminated by using coupled output inductors.<sup>1</sup> ~ K.B.*

The push-pull converter is one of the oldest topologies and is still popular. It can provide multiple outputs whose returns are DC-isolated from input ground and from one another. Output voltages can be higher or lower than the input voltage. The master is regulated against line and load variations. The slaves are equally well regulated against line changes and can be within about 5% for load changes as long as output inductors are not permitted to go discontinuous.

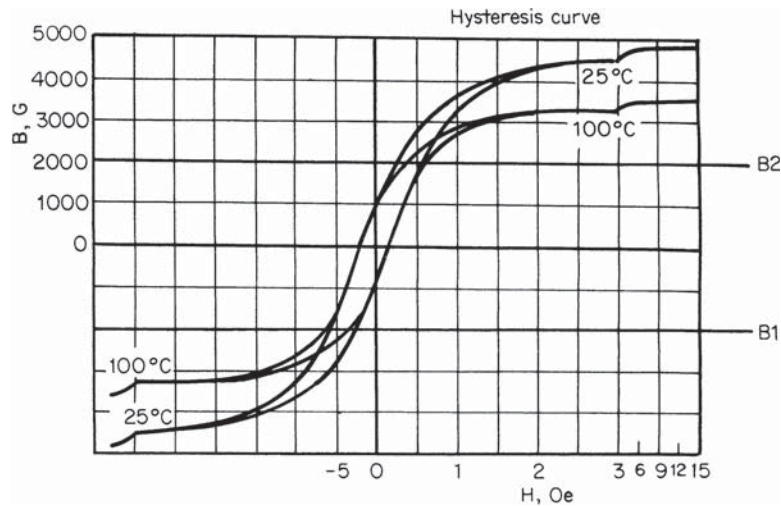
### 2.2.5 Flux Imbalance in the Push-Pull Topology (Staircase Saturation Effects)

The designer needs to be aware of a rather subtle failure mode in push-pull converters, known as *staircase saturation*, caused by a possible flux imbalance in the transformer core.

This effect can best be understood by examination of a typical hysteresis loop of a ferrite core material used in the power transformer as shown in Figure 2.3.

In normal operation, core flux excursions are between levels such as  $B_1$  and  $B_2$  gauss in Figure 2.3. It is important to stay on the linear part of the hysteresis loop below about  $\pm 2000$  G. At frequencies up to 25 kHz or so, core losses are low and these maximum excursions are permissible. As discussed in Section 2.2.9.4, however, core losses go up rapidly with frequency, and above 100 kHz conservative design limits peak flux density to 1200 or even 800 G.

It can be seen in Figure 2.1 that when  $Q_1$  is “on,” the no-dot end of  $N_{p1}$  is positive with respect to the dot end, and the core moves up the hysteresis loop—say, from  $B_1$  toward  $B_2$ . The actual amount it moves up is proportional to the product of the voltage across  $N_{p1}$  and  $Q_1$  “on” time (from Faraday’s law; see Eq. 1.18). When  $Q_1$  turns “off” and  $Q_2$  turns “on,” the dot end of  $N_{p2}$  is positive with respect to the no-dot end, and the core moves back down from  $B_2$  toward  $B_1$ . The actual amount it moves down is proportional to the voltage across  $N_{p2}$  and the  $Q_2$  “on” time.



**FIGURE 2.3** Hysteresis loop of a typical ferrite core material (Ferroxcube 3C8). Flux excursions are generally limited to  $\pm 2000$  G up to about 30 kHz by requirement to stay on the linear part of the loop. At higher frequencies of 100 to 300 kHz, peak flux excursions must be reduced to about  $\pm 1200$  or  $\pm 800$  G because of core losses. Material 3C8 is a ferrite from Ferroxcube Corporation. Other materials from this or other manufacturers are very similar, differing mainly in core losses and Curie temperature.

Further, if the volt-second product across  $N_{p1}$  while  $Q1$  is “on” is equal to the volt-second product across  $N_{p2}$  while  $Q2$  is “on”, after one complete period the core will have moved up from  $B_1$  to  $B_2$  and returned exactly to  $B_1$ . But if those volt-second products differ by only a few percent and the core has not returned to its exact starting point each cycle, after a number of periods the core will “walk” or “staircase” up or down the hysteresis loop into saturation. In saturation, of course, the core cannot sustain voltage, and the next time a transistor turns “on,” it will be destroyed by high current and high voltage.

A number of factors can cause the “on” volt-second product to be different from the “off” or reset volt-second product. The  $Q1$  and  $Q2$  collector voltages and “on” times may not be exactly equal even if their base drive “on” times are equal. If  $Q1$ ,  $Q2$  are bipolar transistors, they have “storage” times that effectively keep the collector “on” after base drive is removed. Storage times can range from 0.3 to 6  $\mu\text{s}$  and have large production spreads. They are also temperature-dependent, increasing significantly as temperature increases. Even if  $Q1$  and  $Q2$  have equal storage times, they may become unequal if located on a heat sink such that they operate at different temperatures.

## 52 Switching Power Supply Design

Hence if one transistor has a volt-second product only slightly larger than the other, it will start the core progressively drifting off-center toward saturation with each cycle. This will cause one transistor to draw slightly more current than the other as the core moves onto the curved part of the hysteresis loop (see Figure 2.3). As a result, the core magnetizing current on that half-period starts to become a significant part of the load current. The transistor that draws more current will now run slightly warmer, increasing its storage time. With a longer storage time in that transistor, the volt-second product it applies to the core in its “on” half period increases, the current in that half period increases, and storage time in that transistor increases still further. Thus a runaway condition arises that quickly drives the core into saturation and destroys the transistor.

The “on” volt-second products of  $Q1$  and  $Q2$  also can differ because of their initially unequal “on” or  $V_{ce(sat)}$  voltages, which have a significant production spread. As described earlier, with bipolar transistors, any initial difference in “on” voltage is magnified because the “on” voltage of bipolars decreases as temperature increases.

If  $Q1$ ,  $Q2$  are MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), the flux-imbalance problem is much less serious. To start with, MOSFETs have no storage time, and with equal input “on” (gate) times, output (drain) times are equal and, importantly, the “on” voltage of a MOSFET transistor increases as temperature increases. Thus the runaway condition described earlier is reversed, providing some compensation. If there were any initial volt-second inequality, one FET current would be greater as the core started moving up the curved part of the hysteresis loop. The FET with the larger current would run warmer, and its “on” voltage would increase and rob voltage from its half primary. This would decrease the volt-second product in that half-period and bring the transistor current back down, providing some compensation.

### 2.2.6 Indications of Flux Imbalance

The earlier description might imply that any slight imbalance in volt-second product between half cycles causes certain failure, but this is not necessarily so. A push-pull converter can continue to operate reliably with a small amount of flux imbalance without immediately saturating its core and destroying its transistors. Many low power, low voltage push-pull converter designs run quite reliably in spite of the apparent problems.

Notice that with a small volt-second imbalance, if there were not an inherent corrective mechanism, core saturation and transistor failure would always occur after a few switching cycles. Thus, if there were an initial volt-second imbalance of say 0.01% (which would be

practically impossible to achieve), it would take only 10,000 cycles until the core would move from a low starting point of  $B_1$  (see Figure 2.3) to a saturating point of  $B_2$ , and the transistors would probably be destroyed before that.

One corrective mechanism, that may permit the converter to survive, is the primary winding resistance. If there is an initial volt-second imbalance, the transistor taking more current produces a larger voltage drop across its half primary winding resistance. That voltage drop robs volt-seconds from the winding and tends to restore the volt-second balance.

Thus the converter can remain in an unbalanced state without immediately going into runaway and completely saturating the core. An indication of where the core is working on the hysteresis loop can be obtained by placing a current probe in the transformer center tap as shown in Figure 2.4d.

The waveform indicating volt-second balance is shown in Figure 2.4a, where alternate current peaks are equal. Primary load current pulses have the characteristic shape of a ramp on a step just as for the buck regulator in Figure 1.4d. They have this shape because all the secondaries have output LC filters that generate such waveshapes as described in Section 1.3.2.

The primary load current is the sum of all the secondary currents reflected into the primary by their respective turn ratios. However, the total primary current is the sum of these secondary currents plus the primary magnetizing current. The magnetizing current is the current drawn by the *magnetizing inductance*, which is the inductance seen looking into the primary with all secondaries open-circuited. This inductance is always present and effectively is in parallel with the primary winding. This current is added to the secondary currents reflected into the primary as in Figure 2.4e.

The waveshape of the total primary current is then the sum of the ramp-on-a-step reflected load currents and the magnetizing current. But providing the core is working in the linear area of the B/H loop, the magnetizing current will be a linear ramp starting from zero current each cycle.

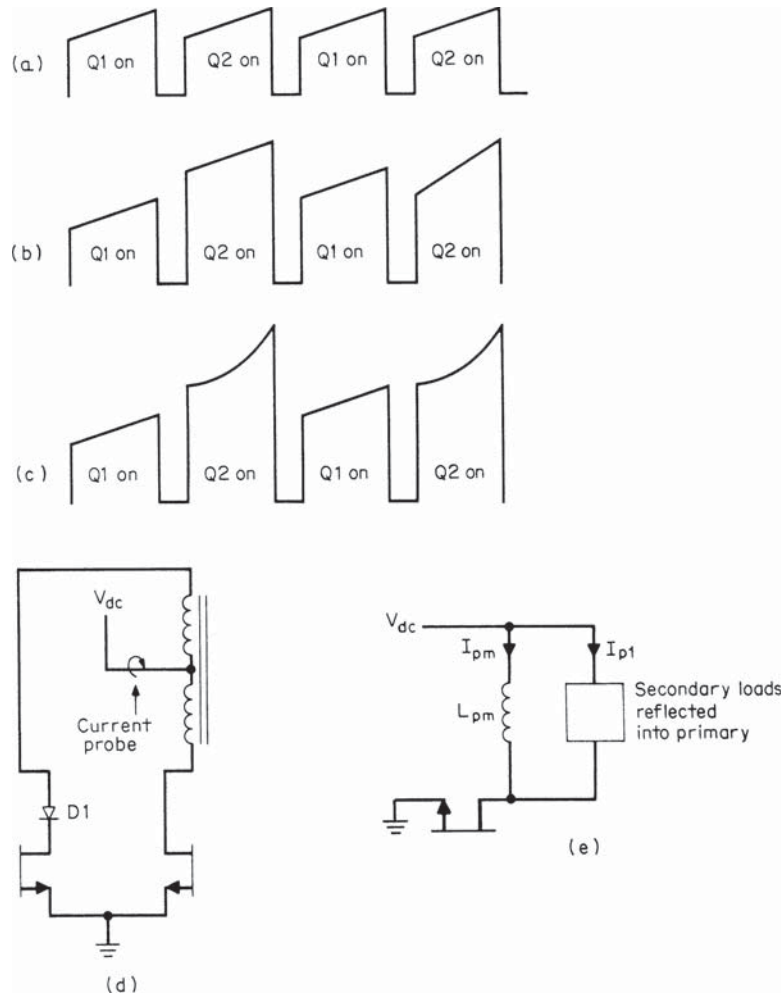
When a transistor turns “on,” it applies a step of voltage of approximately  $V_{dc} - 1$  across the magnetizing inductance  $L_{pm}$ . Magnetizing current then ramps up linearly at a rate

$$dI/dt = (V_{dc} - 1)/L_{pm} \quad (2.4)$$

and for the transistor “on” time of  $T_{on}$  it reaches a peak of

$$I_{pm} = \frac{(V_{dc} - 1)(T_{on})}{L_{pm}} \quad (2.5)$$

## 54 Switching Power Supply Design



**FIGURE 2.4** Current waveforms in the transformer center tap. (a) Waveform shows equal volt-second product on the two halves of transformer primary. (b) Unequal volt-second product on the two halves of transformer primary. Core is not yet on curved part of hysteresis loop. (c) Unequal volt-second product. Upward concavity indicates dangerous situation. Core is far up on curved part of hysteresis loop. (d) Adding a diode in series with one side of primary to test how serious a volt-second inequality exists. (e) Total primary current is the sum of the ramp-on-a-step reflected secondary load currents plus the linear ramp of magnetizing current.

The magnetizing current  $I_{pm}$  is kept small compared with the sum of the load currents reflected into the primary by ensuring that  $L_{pm}$  in Eq. 2.5 is large. By design, the peak magnetizing current should be no greater than 10% of the primary load current.

When added to the ramp-on-a-step load current, the ramp of magnetizing current is small, and it simply increases the slope of the latter slightly. Also, if the volt-seconds are equal on alternate half cycles, the peak currents will also be equal on each half cycle as in Figure 2.4a, because operation is centered around the origin of the hysteresis loop of Figure 2.3.

However, if the volt-second products on alternate half cycles are unequal, core operation is not centered on the origin of the hysteresis loop. Since the horizontal scale ( $H$  oersteds) is proportional to magnetizing current, this shows up as a DC current bias as in Figure 2.4b, making alternate current pulses unequal in amplitude.

As long as the DC bias does not drive the core up the hysteresis loop appreciably, the slope of the ramp still remains linear (Fig. 2.4b) and operation is still reasonably safe. Primary wiring resistance may keep the core from moving further up into saturation.

But if there is a large inequality in volt-seconds on alternate half cycles, the core is biased closer toward saturation and enters the curved part of the hysteresis loop. Now the magnetizing inductance, which is proportional to the slope of the hysteresis loop, decreases and magnetizing current increases significantly. This shows up as an upward concavity in the current slope in Figure 2.4c.

This is a dangerous and imminent failure situation. Now even a small temperature increase can bring on the runaway scenario described earlier. The core will be driven hard into saturation and destroy the power transistor. A push-pull converter design should certainly not be considered safe if current pulses in the primary center tap show any upward concavity in their ramps. Even linear ramps as in Figure 2.4b with anything greater than 20% inequality in peak currents are unsafe and should not be accepted.

**Note** *A more damaging effect can occur if there is a sudden transient load change, because the extra current can take the core immediately into saturation. ~ K.B.*

### 2.2.7 Testing for Flux Imbalance

A simple test to determine how close to a dangerous flux-imbalance situation a push-pull converter may be operating is shown in Figure 2.4d. Here a silicon diode with about 1 V forward drop is placed in series with one half of the transformer primary. Now in the “on” state, that half with the diode in series has 1 V less voltage across it

## 56 Switching Power Supply Design

than the other half, and there is an artificially produced volt-second unbalance. The center tap waveform will then look like either Figure 2.4b or 2.4c. The current ramp corresponding to the side that does not have the diode will have the larger volt-second product and the larger peak current. By switching the diode to the other side, the larger peak current will be seen to switch to the opposite transformer half primary.

Now the closeness of the circuit to the upward concave situation of Figure 2.4c can be determined. If one series diode can make a current ramp go concave, the circuit is too close to imminent failure. Placing two series diodes on one side will give an indication of how much margin there is.

It should be noted that primary magnetizing current contributes no power to the secondaries. It will not appear in the secondaries. It simply swings the magnetic core across the hysteresis loop.

In Figure 2.3, the magnetizing force  $H$  in oersteds (Oe) is related to the current by the fundamental magnetic relation

$$H = \frac{0.4\pi N_p I_m}{l_m} \quad (2.6)$$

where  $N_p$  is the number of primary turns

$I_m$  is the magnetizing current in amperes

$l_m$  is the magnetic path length in cm

### 2.2.8 Coping with Flux Imbalance

Flux imbalance can become a major problem at high voltages and high powers. There are a number of ways to circumvent the problem, but most involve increased cost or component count. Some schemes to combat flux imbalance are described in the following subsections.

#### 2.2.8.1 Gapping the Core

Flux imbalance becomes serious when the core moves out onto the curved part of the hysteresis loop (see Figure 2.3) and magnetizing current starts increasing exponentially as in Figure 2.4c. This effect can be reduced by moving the curved part of the hysteresis loop to a higher current by tilting the hysteresis loop. The core can then tolerate a larger DC current bias or volt-second product inequality.

An air gap introduced into the magnetic path of the core has the effect shown in Figure 2.5. It tilts the slope of the hysteresis loop. An air gap of 2 to 4 mils (thousandths of an inch) brings the curved portion of the loop much further away from the origin so that the core can accept a reasonably large offset in  $H$  (current imbalance). This can help at higher power levels. It has the disadvantage of reducing the inductance so that the critical current must be larger to prevent discontinuous-mode operation.



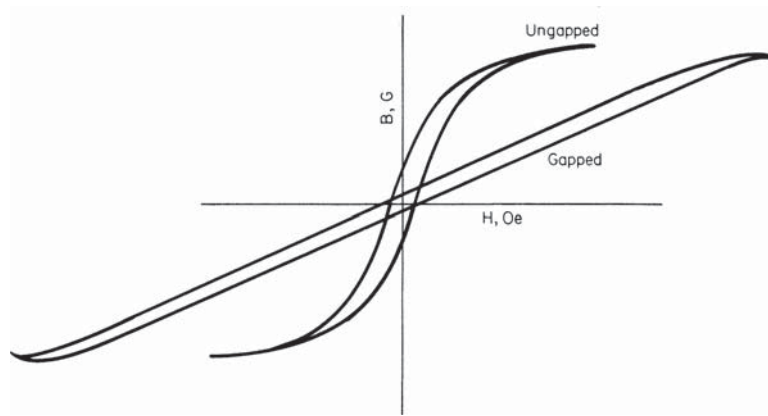


FIGURE 2.5 How a gap in the core reduces the slope of the hysteresis loop.

The air gap for a prototype EE or cup core is easily effected with plastic shims in the center and outer legs. Since the flux passes through the center leg and returns through the outer legs, the total gap is twice the shim thickness. In a production transformer, it is not very much more expensive to have the center leg ground down to twice the shim thickness. This will achieve pretty much the same effect as shims in the center and outer legs, but is preferable as the gap will not change with changes in the thickness of the plastic and results in less magnetic radiation and hence reduced RFI interference.

### 2.2.8.2 Adding Primary Resistance

It was pointed out in Section 2.2.6 that primary wiring resistance keeps the core from being driven rapidly into saturation if there is a volt-second inequality. If there is such an inequality, the half primary with the larger volt-second product draws a larger peak current. That larger current causes a larger voltage drop across the wiring resistance and robs volt-seconds from that half primary, restoring the current balance.

This effect can be augmented by adding additional resistance in series with both primary halves. The added resistors can be located in either the collectors or emitters of the power transistors. The value is best determined empirically by observing the current pulses in the transformer center tap. The required resistors are usually under  $0.25\ \Omega$ . They will, of course, increase power loss and reduce efficiency.

### 2.2.8.3 Matching Power Transistors

Since volt-second inequality arises mainly from an inequality in storage time or voltage in the power transistors, if those parameters are



## 58 Switching Power Supply Design

matched, it adds confidence that together with the earlier two “fixes” there will be no problem with flux imbalance.

This is not a good solution and would be an expensive fix as it is quite expensive to match transistors in two parameters. To do such matching requires a specialized test setup that would not be available if field replacements become necessary.

It also must be ascertained that if the matching is done at certain load currents and temperature, the matching still holds when these vary. Further, a storage time match is difficult to make credible, as it depends strongly on forward and reverse base input currents in the bipolar transistors. Generally any matching is done by matching  $V_{ce}$  and  $V_{be}$  (the “on” collector-to-emitter and base-to-emitter voltages) at the maximum operating current. Hence matching is not a viable solution for high-volume commercial supplies.

### 2.2.8.4 Using MOSFET Power Transistors

Since most of the volt-second inequality arises from storage time inequality between the two bipolar power transistors, the problem largely disappears if MOSFETs are used, because they have no storage time.

There is an added advantage, as the “on” voltage of a MOSFET transistor increases with temperature. Thus if one half primary tends to take a large current, its transistor runs somewhat warmer and its “on” voltage increases and steals voltage from the winding. This reduces the volt-second product on that side and tends to restore balance. This, of course, is qualitatively in the right direction, which is helpful but cannot be depended on to solve the flux-imbalance problem reliably at all power levels and with a worst-case combination.

However, with power MOSFETs at power levels under 100 W and low input voltages (as in most DC/DC converter applications), push-pull converters can be and are built with a high degree of confidence.

### 2.2.8.5 Using Current-Mode Topology

By far the best solution to the flux-imbalance problem is to use current-mode control. This completely and reliably solves the flux-imbalance problem; also it has significant additional advantages of its own.

In conventional push-pull, there is always a residual concern that despite all the fixes, a flux-imbalance problem will arise in some worst-case situation and a transistor will be destroyed. Current-mode topology solves this problem by monitoring the current in each of the push-pull transistors on a pulse-by-pulse basis. The control circuit then forces alternate current pulses to have equal amplitude, maintaining the working point very near the center of the B/H loop. Details of current-mode topology will be discussed in Chapter 5.

### 2.2.9 Power Transformer Design Relationships

**Note** *The design of wound components is a specialized subject and is covered in more detail in Chapter 7. The correct design of transformers, inductors, and chokes is essential for optimum performance of the equipment. The engineer who takes the time to become fully competent in this area will get much better results, so the reader is urged to study Chapter 7 before proceeding with any real designs.*

**After Pressman** *In the following section Mr. Pressman shows an iterative method for selecting the core size and winding parameters. It serves as a good example of the rather lengthy process required if this method is used. The reader will do well to study this process, which shows the interaction between the various parameters. However, in practice, optimum designs normally start by defining the maximum permitted temperature rise (typically 30°C), and one of the nomogram-assisted methods or computer programs would be used to provide a much faster solution with a defined result, avoiding the tedious iterative procedure. ~ K.B.*

#### 2.2.9.1 Core Selection

The design of a transformer starts with the initial selection of a core to satisfy the desired total output power. The available output power from a particular core depends on the operating frequency, the operating flux density swing ( $B_1$  and  $B_2$  in Figure 2.3), the core's area  $A_e$ , the bobbin winding window area  $A_b$ , and the current density in each winding.

Decisions on each of these parameters are interrelated, and choices are made to minimize the transformer size and its temperature rise. In the magnetics section of Chapter 7 an equation is derived showing a recommended output power for a given core as a function of the parameters mentioned earlier.

The equation can be used in a set of iterative calculations, first making a tentative selection of a specific core, peak flux density, and operating frequency, and calculating the available output power. Then if the available power is insufficient, a larger-sized core is selected and the calculations repeated until a core with the required output power is found.

This is a long and cumbersome procedure; instead the equation is turned into a set of charts that permit a core and operating frequency to be selected at a glance for any desired output power. Such equations and charts will be found for most of the commonly used topologies in Chapter 7.

## 60 Switching Power Supply Design

We will assume that these charts will be used to select a specific core so that the area  $A_e$  is known. The rest of the transformer design involves calculation of the number of turns on the primary and secondaries, selection of wire sizes, calculation of core and copper losses, and finally the calculation of transformer temperature rise.

The optimum arrangement of the various layers of wire on the core bobbin is important in improving coupling between the windings and in reducing copper losses due to “skin” and “proximity” effects. Winding arrangements, skin, and proximity effects will be discussed in Chapter 7.

For this example, the design will proceed using the core chosen from the selection charts described earlier, providing a known value of the core area  $A_e$ .

### 2.2.9.2 Maximum Power Transistor On-Time Selection

Equation 2.1 has shown that the converter keeps the output voltage  $V_m$  constant by increasing  $T_{on}$  as  $V_{dc}$  decreases. Thus the maximum “on” time  $T_{on}$  occurs at the *minimum* specified DC input voltage  $V_{dc}$ . But in this type of converter the maximum “on” time must not exceed half the switching period  $T$ . If it were to do so, the reset volt-second product would be less than the set volt-second product (see Section 2.2.5), and after a very few cycles, the core would drift into saturation and destroy a power transistor.

Moreover, because of the inevitable storage time in bipolar transistors, the base drive “on” time cannot be as large as a full half period, as the storage time would cause an overlap with the opposite transistor. This would result in immediate failure, because the two power transistors would effectively short out the winding. Each transistor would take large currents at the full supply voltage and would rapidly be destroyed.

Thus, to ensure that the core will always be reset within one period and eliminate any possibility of simultaneous conduction, whenever the DC input voltage is at its minimum  $V_{dc}$  and the feedback loop is trying to increase  $T_{on}$  to maintain  $V_m$  constant, the maximum “on” time will be constrained by some kind of a clamp so as to never be more than 80% of a half period. Then in Eq. 2.1, for the specified  $V_{dc}$ ,  $T$  and for  $\overline{T_{on}} = 0.8T/2$ , the ratio  $N_m/N_p$  will be fixed to yield the desired output  $V_m$ .

**TIP** Modern drive and control ICs provide adjustable (so-called) “dead time” to prevent power device overlap. In some designs, dynamic methods are provided such that the state of conduction of the power devices is monitored and the drive signal is delayed until the previous active power device has turned fully “off,” before the next is allowed to turn “on.” This allows the full

## Chapter 2: Push-Pull and Forward Converter Topologies 61

range of duty cycle to be utilized while completely eliminating any possibility of overlap. ~ K.B.

### 2.2.9.3 Primary Turns Selection

The number of primary turns is determined by Faraday's law (see Eq. 1.17). From it  $N_p$  is fixed by the minimum voltage across the primary ( $V_{dc} - 1$ ) and the maximum "on" time, which, as earlier, is to be no more than  $0.8T/2$ . Then

$$N_p = \frac{(V_{dc} - 1)(0.8T/2) \times 10^8}{A_e dB} \quad (2.7)$$

Since  $A_e$  in Eq. 2.7 is fixed by the selected core,  $V_{dc}$  and  $T$  are specified and the number of primary turns is fixed as soon as  $dB$  (the desired flux change in  $0.8T/2$ ) is decided on. This decision is made as follows.

**TIP** The reader may prefer to use a dimensionally modified version of Faraday's law that provides turns directly as follows:

$$N = \frac{VT_{on}}{A_e \Delta B}$$

Where  $N$  = turns

$V$  = voltage across the winding ( $V_{dc}$ )

$T_{on}$  = maximum "on" period, microseconds

$\Delta B$  = flux density swing, teslas (1 tesla = 10,000 gauss)

$A_e$  = effective core area,  $mm^2$

For all magnetic calculations, I prefer to work in the preceding modified SI units, as these yield immediate solutions, avoiding the unwieldy exponents, thus reducing errors. ~ K.B.

### 2.2.9.4 Maximum Flux Change (Flux Density Swing) Selection

From Eq. 2.7, it is seen that the number of primary turns is inversely proportional to  $dB$ , the flux swing. It would seem desirable to maximize  $dB$  so as to minimize  $N_p$ , since fewer turns would mean that a larger wire size could be used, resulting in higher permissible currents and more output from a given core. Also, fewer turns would result in a less expensive transformer and lower stray parasitic capacities.

From the hysteresis loop of Figure 2.3, however, it is seen that in ferrite cores, the loop enters the curved portion above  $\pm 2000$  G. It is desirable to stay below this point, where the magnetizing current starts increasing rapidly. So initially a good choice would appear to be  $\pm 2000$  G (0.2 tesla). But we must also consider core losses.

Ferrite core losses increase at about the  $2.7^{th}$  power of the peak flux density and at about the  $1.6^{th}$  power of the operating frequency.

## 62 Switching Power Supply Design

Hence, up to about 50 kHz, core losses do not prohibit operation to  $\pm 2000$  G, and it may appear desirable to operate at that flux level.

However, to prevent core saturation under transient conditions, it is better to provide a wider margin. We will see shortly that it is preferable to restrict operation to  $\pm 1600$  G even at frequencies where core losses are not prohibitive. Faraday's law solved for the flux change  $dB$  is

$$dB = \frac{(V_{dc} - 1)(T_{on}) \times 10^8}{N_p A_e} \quad (2.8)$$

Equation 2.8 says that if  $N_p$  is chosen for a given  $dB$ —say, from  $-2000$  to  $+2000$  G, or a  $dB$  of  $4000$  G, then as long as the product of  $(V_{dc} - 1)(T_{on})$  is constant,  $dB$  will be constant at  $4000$  G. Further, if the feedback loop is working and keeping the output voltage  $V_m$  constant, Eq. 2.1 says that  $(V_{dc} - 1)(T_{on})$  is constant and  $dB$  will truly remain constant. So providing the feedback loop always ensures that whenever  $V_{dc}$  is a minimum, that  $T_{on}$  is at a maximum, then  $T_{on}$  and  $V_{dc}$  can never be simultaneously maximum.

However, in some transient or fault conditions, if  $T_{on}$  has been at maximum for a single, or possibly even a few cycles, and  $V_{dc}$  had a transient step to 50% above its normal value, the feedback loop may fail to reduce the “on” time rapidly enough (as normally required by Eq. 2.1), and there may exist a short period when  $V_{dc}$  and  $T_{on}$  would be maximum at the same time. In this event, Equation 2.8 shows that  $dB$  would be  $1.5(4000)$  or  $6000$  G.

Then if the core had started from the  $-2000$ -G point, at the end of that “on” time the core would have been driven  $6000$  G above that, or to  $+4000$  G. The hysteresis loop (see Figure 2.3) shows that at temperatures somewhat above  $25^\circ\text{C}$ , it would be deep in saturation and could not support the applied voltage. The transistor would be subject to high current and high voltage and would rapidly fail.

It will be seen in the feedback analysis section of Chapter 12 that the error amplifier has a delay in its response time, because its bandwidth is limited to stabilize the feedback loop. Hence, it is always possible for both the input voltage and “on” time to be maximum for a transient period due to the inevitable delay in the response of the error amplifier, although the error amplifier will eventually correct the “on” time so as to keep the product  $(V_{dc} - 1)(T_{on})$  constant in accordance with Eq. 2.1. If the core is subjected to maximum input voltage and maximum “on” time as a result of error-amplifier delay, even for a single cycle, it may saturate the core and destroy a transistor.

However if  $N_p$  in Eq. 2.8 is chosen to yield  $dB$  of  $3200$  G at  $V_{dc}$  and  $T_{on}$ , the design is safer and can tolerate a 50% transient step in input voltage. With  $dB = 3200$  G, if the error amplifier is too slow to correct

the “on” time, the transformer  $dB$  will be  $1.5(3200)$  or  $4800$  G; and if the core started from its normal minimum flux of  $-1600$  G, it will be driven up to only  $-1600 + 4800$  or  $+3200$  G. The hysteresis loop of Figure 2.3 shows that the core can tolerate that even at  $100^\circ\text{C}$ .

Thus the number of primary turns is selected from Eq. 2.7 for  $dB = 3200$  G even at lower frequencies where a large flux may not cause excessive core losses. Above  $50$  kHz, the core losses increase rapidly and force a lower flux density selection. At  $100$  to  $200$  kHz, the peak flux density may be limited to  $1200$  or even  $800$  G to achieve an acceptably low core temperature rise.

### 2.2.9.5 Secondary Turns Selection

The turns for the main and slave outputs are calculated from Eqs. 2.1, 2.2, and 2.3 in accordance with the specified, or calculated, voltage requirements. We see that the input voltage  $V_{dc}$  and  $T$  have been specified. The maximum “on” time  $T_{on}$  has been arbitrarily set at  $0.8T/2$ , and  $N_p$  has been calculated from Faraday’s law (see Eq. 2.7) for the known  $A_e$  for the selected core. Flux swing  $dB$  has been set at  $3200$  G for frequencies under  $50$  kHz and to minimize core losses. Lower values will be used at higher frequencies as discussed earlier.

### 2.2.10 Primary, Secondary Peak and rms Currents

In this example, wire sizes will be selected on the basis of a conservative operating current density. Current density is given in terms of rms current in amps per circular mil\* of wire cross-sectional area.

Hence, before we can start selecting wire sizes for any winding, we require a knowledge of the rms currents in each winding.

#### 2.2.10.1 Primary Peak Current Calculation

Current drawn from the DC input source  $V_{dc}$  may be monitored in the transformer center tap and has the waveform shown in Figures 2.1b and 2.1d. The pulses have the characteristic ramp-on-a-step wave-shape because the secondaries all have output  $LC$  filters as discussed in Section 1.3.2. The primary current is simply the sum of all the secondary ramp-on-a-step currents reflected into the primary by their turns ratios, plus the magnetizing current.

As discussed in Section 2.2.9.2, at minimum  $V_{dc}$  input voltage, the transistor “on” times will be  $80\%$  of a half period. Further, since there is one pulse for each half period, the duty cycle of the pulses in Figure 2.1

\*A circular mil is the area of a circle 1 mil in diameter. Thus, area in square inches  $= (\pi/4)10^{-6}$  (area in circular mils).

## 64 Switching Power Supply Design

is 0.8 at  $V_{dc}$ . To simplify calculation, the pulses in the figure are assumed to have an equivalent flat-topped waveshape whose amplitude  $I_{pft}$  is the value of the current at the center of the ramp.

Then the input power at  $V_{dc}$  is that voltage times the average current, which is  $0.8I_{pft}$ , and assuming 80% efficiency (which is usually achievable up to 200 kHz),  $P_o = 0.8P_{in}$  or

$$P_{in} = 1.25P_o = \frac{V_{dc}}{0.8}I_{pft}$$

Then

$$I_{pft} = 1.56 \frac{P_o}{V_{dc}} \quad (2.9)$$

This is a useful relation, as it gives the equivalent flat-topped primary current pulse amplitude in terms of what is known—the output power and the specified minimum DC input voltage. It allows selection of a primary wire size from the calculated primary rms current. It also allows a transistor with an adequate current rating to be selected.

### 2.2.10.2 Primary rms Current Calculation and Wire Size Selection

Each half primary carries only one of the  $I_{pft}$  pulses per period, and hence its duty cycle is  $(0.8T/2)/T$  or 0.4. It is well known that the rms value of a flat-topped pulse of amplitude  $I_{pft}$  at a duty cycle  $D$  is

$$I_{rms} = I_{pft}\sqrt{D} = I_{pft}\sqrt{0.4}$$

or

$$I_{rms} = 0.632I_{pft} \quad (2.10)$$

and from Eq. 2.9

$$I_{rms} = 0.632 \frac{1.56P_o}{V_{dc}} = \frac{0.986P_o}{V_{dc}} \quad (2.11)$$

This gives the rms current in each half primary in terms of the known parameters: output power and the specified minimum DC input voltage.

A conservative practice in transformer design is to operate the windings at a current density of 500 circular mils per rms ampere. There is nothing absolute about this; current densities of 300 circular mils per rms ampere are frequently used for windings with only a few turns. As a general rule, however, densities greater than 300 circular mils per rms ampere should be avoided, as that will cause excessive copper losses and temperature rise.



## Chapter 2: Push-Pull and Forward Converter Topologies 65

Thus at 500 circular mils per rms ampere, the required number of circular mils for the half primaries is

$$\begin{aligned}\text{Circular mils} &= 500 \frac{0.986 P_o}{V_{dc}} \\ &= 493 \frac{P_o}{V_{dc}}\end{aligned}\quad (2.12)$$

Notice that this is also in terms of known values—output power and specified minimum DC input voltage. Proper wire size can then be chosen from wire tables at the circular mils given by Eq. 2.12.

### 2.2.10.3 Secondary Peak, rms Current, and Wire Size Calculation

Currents in each half secondary are shown in Figure 2.6. Note the ledge at the end of the transistor “on” time. This ledge of current exists because there is no free-wheeling diode  $D1$  at the input to the filter inductor as in the buck regulator of Figure 1.4. In the buck, the free-wheeling diode was essential as a return path for inductor current when the transistor turned off. When the transistor turned off, the polarity across the output inductor reversed, and its input end would have gone disastrously negative if it had not been caught by the free-wheeling diode at about 1 V below ground. Inductor current then continued to flow through the free-wheeling diode  $D1$  of Figure 1.4e. This problem does not exist in the rectifier circuit shown in Figure 2.6.

In the push-pull output rectifier stage, the function of the free-wheeling diode is performed by the output rectifier diodes  $D1$  and  $D2$ . When either transistor turns “off,” the input end of the inductor tries to go negative. As soon as it goes about one diode drop below ground, both rectifiers conduct, each drawing roughly half the total current the inductor had been drawing just prior to turn “off” (see Figures 2.6d and 2.6e). Since the impedance of each half secondary is small, there is negligible drop across them, and the rectifier diode cathodes are caught at about 1 V below ground.

Thus if half-secondary rms currents are to be calculated exactly, the ledge currents during the 20% dead time should be taken into account. However, in this example it can be seen that they are only about half the peak inductor current and have a duty cycle of  $(0.4T/2)/T$  or 0.2. With such small amplitudes and duty cycle they can be ignored in this example. Each half secondary can then be considered to have the characteristic ramp-on-a-step waveform, which at minimum DC input comes out to a duty cycle of  $(0.8T/2)/T$  or 0.4. The magnitude of the current at the center of the ramp is the DC output current  $I_{dc}$ , as can be seen from Figure 2.6f.



## 66 Switching Power Supply Design

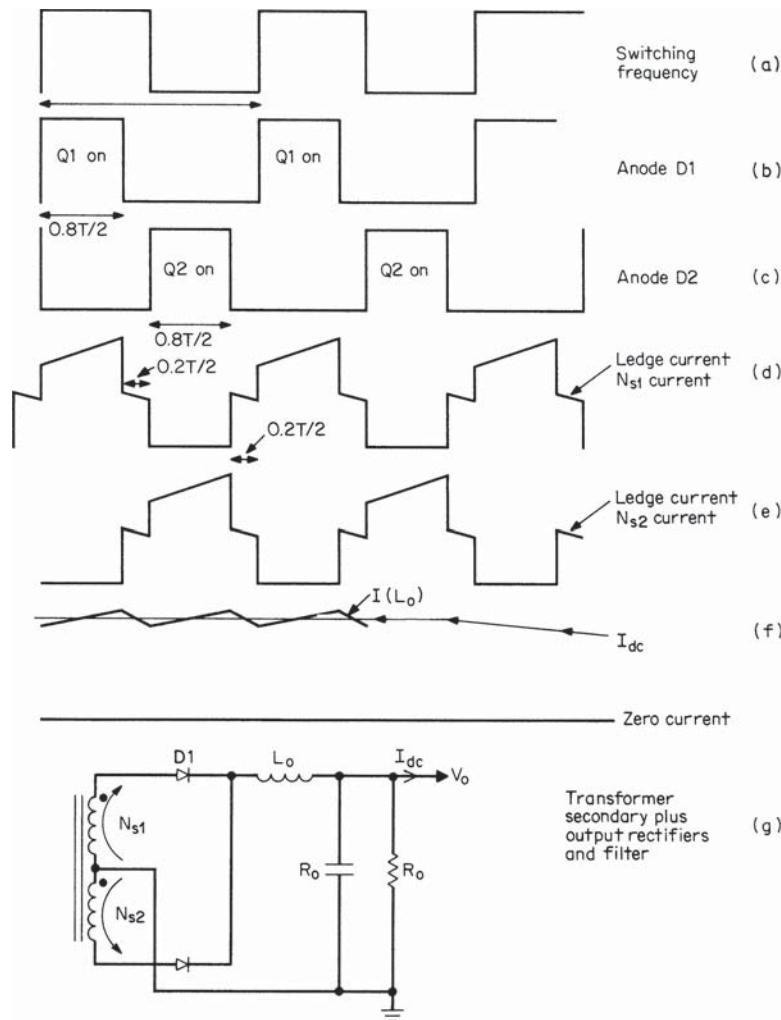


FIGURE 2.6 Output rectifiers  $D1$  and  $D2$  serve as free-wheeling diodes in a push-pull rectifier circuit. Each secondary winding carries half the normal free-wheeling “ledge” during the 20% dead time. This should be considered in estimating secondary copper losses.

### 2.2.10.4 Primary rms Current, and Wire Size Calculation

To simplify the primary current rms calculations, the ramp-on-a-step pulses will be approximated by “equivalent flat-topped” pulses  $I_{aft}$ , whose amplitude is that at the center of the ramp or the DC output current  $I_{dc}$  with a duty cycle of 0.4.

## Chapter 2: Push-Pull and Forward Converter Topologies 67

Thus rms current in each half secondary is

$$I_{s(\text{rms})} = I_{\text{dc}}\sqrt{D} = I_{\text{dc}}\sqrt{0.4} = 0.632I_{\text{dc}} \quad (2.13)$$

At 500 circular mils per rms ampere, the required number of circular mils for each half secondary is

$$\begin{aligned} \text{Secondary circular mil requirement} &= 500(0.632)I_{\text{dc}} \\ &= 3.16I_{\text{dc}} \end{aligned} \quad (2.14)$$

### 2.2.11 Transistor Voltage Stress and Leakage Inductance Spikes

It can be seen from the polarities of the transformer primary windings in Figure 2.1 that when either transistor is “on,” the opposite transistor’s collector is subject to at least twice the DC supply voltage, since both half primaries have an equal number of turns and are in series, with the center tap connected to the supply.

However, the maximum stress is somewhat more than twice the input voltage. An additional contribution comes from the so-called leakage inductance spikes shown in Figures 2.1a and 2.1c. These come about because there is effectively a small inductance (leakage inductance  $L_l$ ) in series with each half primary as shown in Figure 2.7a.

At the instant of turn “off,” current in the transistor falls rapidly at a rate  $dI/dT$ , causing a positive-going spike of amplitude  $e = L_l dI/dT$  at the bottom end of the leakage inductance. Conservative design practice assumes the leakage inductance spike may increase the stress voltage by as much as 30%, more than twice the maximum DC input voltage. Hence the transistors should be chosen so that they can tolerate with some safety margin a maximum voltage stress  $V_p$  of

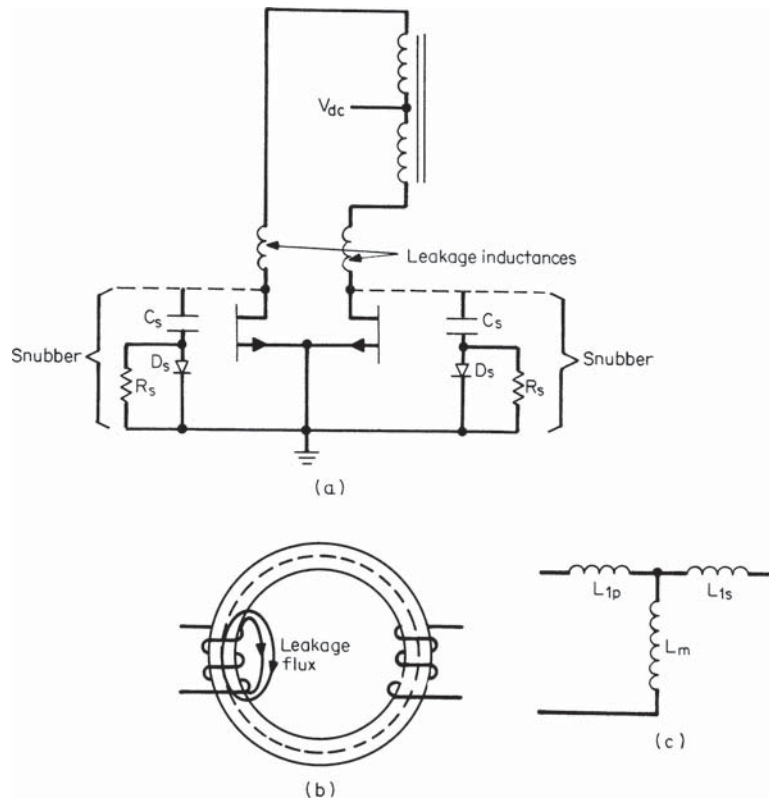
$$V_p = 1.3(2V_{\text{dc}}) \quad (2.15)$$

The magnitude of the leakage inductance is not easily calculable. It can be minimized by use of a transformer core with a long center leg and by sandwiching the secondary windings (especially the higher current ones) in between halves of the primary. A good transformer should have leakage inductance of no more than 4% of its magnetizing inductance.

**TIP** *The leakage inductance of any winding can be easily measured by short-circuiting all other windings and measuring the residual inductance on the required winding. ~ K.B.*

Leakage inductance spikes can be minimized by addition of a snubber circuit (a capacitor, resistor, and diode combination) connected to the transistor collector as shown in Figure 2.7a. Such

## 68 Switching Power Supply Design



**FIGURE 2.7** (a) How leakage inductances cause spikes on the collectors of the power devices. (b) How leakage inductance stems from the fact that some of the magnetic flux lines return through a local air path rather than linking the secondary through the core. (c) The low-frequency equivalent circuit of a transformer showing magnetizing inductance  $L_m$  and primary and secondary leakage inductances  $L_{1p}$ ,  $L_{1s}$ .

configurations also serve the important function of reducing AC switching losses by load line shaping (phase shifting the overlap of falling transistor current and rising voltage at the collector). Detailed design of snubbers and some associated penalties they incur are discussed in Chapter 11.

Leakage inductance arises from the fact that some of the primary's magnetic flux lines do not return through the core and couple with the secondary windings. Instead, they return around the primary winding through a local air path as seen in Figure 2.7b.

The equivalent circuit of a core with its magnetizing  $L_m$  (see Section 2.2.6) and primary  $L_{1p}$  leakage inductances is shown in Figure 2.7c.

Secondary leakage inductance arises from the fact that some of the secondary current's magnetic flux lines also do not couple with the primary but instead link the secondary windings via a local air path. But in most cases, there are fewer turns on the secondary than on the primary, and  $L_{1s}$  can be neglected.

The transformer equivalent circuit shown in Figure 2.7c is a valuable tool in the understanding of many unexpected circuit effects and can be used up to about 300 to 500 kHz, where shunt parasitic capacitors across and between windings must also be taken into account.

## 2.2.12 Power Transistor Losses

### 2.2.12.1 AC Switching or Current-Voltage "Overlap" Losses

Leakage inductance in the power transformer allows a very rapid collector voltage fall time because for a short time when a transistor turns on, the leakage inductance has a very high impedance. Since the current cannot change instantaneously through an inductor, the collector current rises slowly during the turn "on" edge. Thus there is very little overlap of falling voltage and rising current at turn "on" and negligible switching loss.

At turn "off," however, the inductance tends to maintain the previous current constant. Hence there is significant overlap and a worst-case scenario may be assumed, such as that shown for the buck regulator of Figure 1.5b. The exact situation is shown in Figure 2.8,

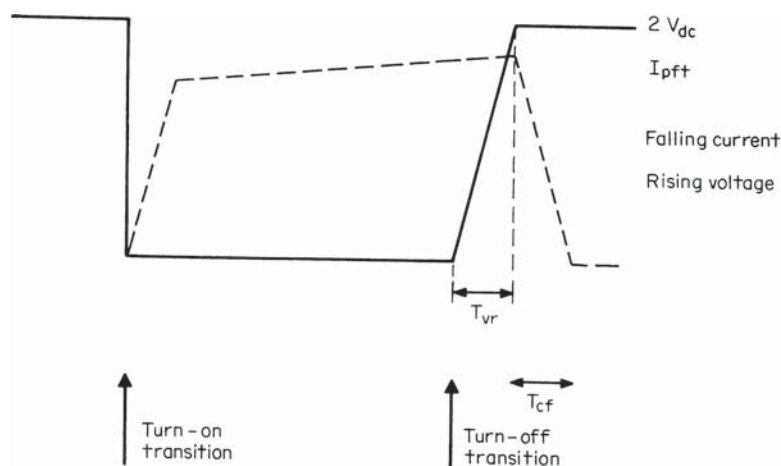


FIGURE 2.8 Switching loss due to current/voltage overlap.

## 70 Switching Power Supply Design

where it is assumed that the current hangs on at its equivalent flat-topped peak value  $I_{\text{pft}}$  (see Section 2.2.10.1) for the time it takes the voltage to rise from near zero to its maximum value of  $2\overline{V_{\text{dc}}}$ . The voltage then remains at  $2\overline{V_{\text{dc}}}$  during the time,  $T_{\text{cf}}$ , it takes the current to fall from  $I_{\text{pft}}$  to zero. Assuming  $T_{\text{vr}} = T_{\text{cf}} = T_s$  and a switching period  $T$ , the total switching dissipation per transistor per period  $P_{t(\text{ac})}$  is

$$\begin{aligned} P_{t(\text{ac})} &= I_{\text{pft}} \frac{2\overline{V_{\text{dc}}}}{2} \frac{T_s}{T} + 2\overline{V_{\text{dc}}} \frac{I_{\text{pft}}}{2} \frac{T_s}{T} \\ &= 2(I_{\text{pft}})(\overline{V_{\text{dc}}}) \frac{T_s}{T} \end{aligned}$$

and from Eq. 2.9,  $I_{\text{pft}} = 1.56(P_o/\underline{V_{\text{dc}}})$ :

$$P_{t(\text{ac})} = 3.12 \frac{P_o}{\underline{V_{\text{dc}}}} \overline{V_{\text{dc}}} \frac{T_s}{T} \quad (2.16)$$

Notice there are negligible switching losses at turn “on” because transformer leakage inductance causes a very fast voltage fall and a slow current rise. This results in very little turn “on” loss. However, worst-case scenario is shown at turn “off.” The current remains constant at its peak  $I_{\text{pft}}$  until voltages rises to  $2\overline{V_{\text{dc}}}$ . The voltage remains at  $2\overline{V_{\text{dc}}}$  for the duration of the current fall time  $T_{\text{cf}}$ , producing a large turn “off” loss.

### 2.2.12.2 Transistor Conduction Losses

The conduction losses are simply the transistor “on” voltage multiplied by the “on” current for each device averaged over a cycle, or

$$P_{\text{dc}} = I_{\text{pft}} V_{\text{on}} \frac{0.8T/2}{T} = 0.4 I_{\text{pft}} V_{\text{on}}$$

It will be seen in Chapter 8 that a technique called *Baker clamping* can be used to reduce transistor storage times for bipolar base drives. This forces the collector “on” potential  $V_{\text{ce}}$  to be about 1 V over a large range of current. Then for  $I_{\text{pft}}$  from Eq. 2.9 we obtain

$$P_{\text{dc}} = 0.4 \frac{1.56 P_o}{\underline{V_{\text{dc}}}} = \frac{0.624 P_o}{\underline{V_{\text{dc}}}} \quad (2.17)$$

and total losses per transistor are

$$\begin{aligned} P_{\text{total}} &= P_{t(\text{ac})} + P_{\text{dc}} \\ &= 3.12 \frac{P_o}{\underline{V_{\text{dc}}}} \overline{V_{\text{dc}}} \frac{T_s}{T} + \frac{0.624 P_o}{\underline{V_{\text{dc}}}} \end{aligned} \quad (2.18)$$

### 2.2.12.3 Typical Losses: 150-W, 50-kHz Push-Pull Converter

It will be instructive to calculate the dissipation per transistor in a 150-W push-pull converter at 50 kHz operating from a 48-volt power source.

The standard telephone industry power sources provide a nominal voltage of 48 V, with a minimum ( $V_{dc}$ ) of 38 V and maximum ( $\overline{V_{dc}}$ ) of 60 V. It will be assumed that at 50 kHz, bipolar transistors will be used, and a reasonable value of the switching time ( $T_s$  as defined earlier) of 0.3  $\mu$ s.

The DC conduction losses from Eq. 2.17 are

$$P_{dc} = \frac{0.624 \times 150}{38} = 2.46 \text{ W}$$

but the AC switching losses from Eq. 2.16 are much larger at

$$P_{t(ac)} = 3.12 \times \frac{150}{38} \times 60 \times \frac{0.3}{20} = 11.8 \text{ W}$$

Thus the AC overlap or switching losses are about 4.5 times greater than the DC conduction losses. If MOSFET transistors are considered with switching times  $T_s$  of about 0.05  $\mu$ s, it can be seen that switching losses would be negligible in this example.

### 2.2.13 Output Power and Input Voltage Limitations in the Push-Pull Topology

Aside from the flux-imbalance problem in the push-pull topology, which does not exist in the current-mode controlled version, limitations include the useful power working area as defined in Eq. 2.9, and input voltage in Eq. 2.15.

Equation 2.9 gives the peak current required of the transistor for a desired output power, and Eq. 2.15 gives the maximum voltage stress on the transistor in terms of the maximum DC input voltage. These requirements limit the power rating of the push-pull topology to around 500 W when using bipolar transistors. Above that, it is difficult to find transistors that can meet the peak current and voltage stress while being fast enough with adequate gain.

The technology is constantly improving, and without doubt a faster MOSFET with adequately high voltage and current ratings and sufficiently low "on" voltages would extend this power range.

As an example, we will consider a 400-W push-pull converter operating from telephone industry prime voltage source that is 48 V (nominal), 38 V (minimum), and 60 V (maximum).

## 72 Switching Power Supply Design

Equation 2.9 gives the peak current requirement as  $I_{\text{pft}} = 1.56P_o/V_{\text{dc}} = 1.56(400)/38 = 16.4$  A, and Eq. 2.15 gives the maximum “off” voltage stress as  $V_p = 2.6V_{\text{dc}} = 2.6 \times 60 = 156$  V. To provide a margin of safety, a transistor with at least a 200-V rating would be selected.

A possible candidate would be the MJ13330 bipolar transistor. It has a 20-A peak current rating, a  $V_{\text{ceo}}$  rating of 200 V, and  $V_{\text{cer}}$  rating of 400 V (the voltage it can sustain when it has a negative bias of  $-1$  to  $-5$  V at turn “off”). It can thus meet the peak voltage and current stresses.

At 16 amps, it has a maximum “on” saturation voltage of about 3 V, a minimum gain of about 5, and a storage time of 1.3 to 4  $\mu\text{s}$ . However, with these limitations, it would have high DC and AC switching losses, have difficulty with flux imbalance (unless the current-mode version of push-pull were used), and would have difficulty operating above 40 kHz because of the long storage times.

A potential MOSFET for such an application is the MTH30N20. This is a 30-A, 200-V device that at 16 A would have only 1.3 V “on” state voltage drop and hence half the DC conduction losses of the preceding bipolar transistor. With its fast switching times it would have quite low switching losses, but this and similar devices can be quite expensive.

For offline converters, the push-pull topology is not very attractive due to the large voltage stress of  $2.6V_{\text{dc}}$  (see Eq. 2.15). For example, with a 120-V AC line input and  $\pm 10\%$  tolerance, the peak rectified DC voltage is  $1.41 \times 1.1 \times 120 = 186$  V. Hence during turn “off” at the top of the leakage spike, Eq. 2.15 gives a peak stress of  $2.6 \times 186 = 484$  V.

We must also allow for transients in the supply above the maximum steady-state values. Transients are seldom specified for commercial power supplies, but conservative design practice assumes stress at least 15% above the maximum steady-state value, increasing the maximum stress to  $1.15 \times 484$  or 557 V.

Input voltage transients in special cases can be even greater, for example, the specifications on military aircraft given by Military Standard 704. Here the nominal voltage is 113 V AC but with a 10-ms transient to 180 V AC, the peak “off” stress from Eq. 1.42 would be  $180 \times 1.41 \times 2.6$  or 660 V. Although there are many fast bipolar transistors that can safely sustain voltages as high as 850 V with reverse input bias, clearly it is not good practice to use a topology that subjects the transistors to high voltage transients.

Some topologies subject the transistors to only the normal maximum DC input voltage stress with no leakage spike. These are a better choice for high voltage and “offline” applications, not only because of the lesser voltage stress, but also because the smaller voltage excursion at turn “off” produces less EMI (electromagnetic interference).

## 2.2.14 Output Filter Design Relations

### 2.2.14.1 Output Inductor Design

It was pointed out in Section 2.2.4 that in both master and slave outputs, the output inductors should not be permitted to go discontinuous. Remember, the discontinuous-mode situation commences at the critical current where the inductor current ramp of Figure 1.6b has dropped to zero. This occurs when the DC current has dropped to half the ramp amplitude  $dI$  (see Section 1.3.6). Then

$$dI = 2\underline{I}_{dc} = V_L \frac{T_{on}}{L_o} = (V_1 - V_o) \frac{T_{on}}{L_o} \quad (2.19)$$

Figure 2.9 shows the output rectifier circuit for calculation of  $L_o$ ,  $C_o$ . When  $V_{dc}$  is at its minimum,  $N_s$  will be chosen so that as  $V_1$  is at its

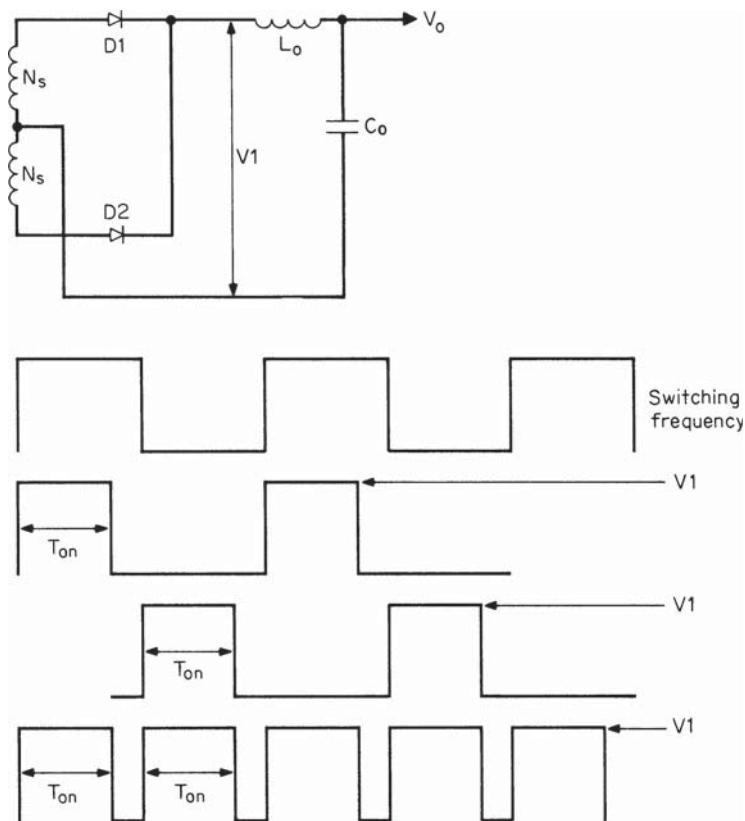


FIGURE 2.9 Output rectifier circuit and waveforms.



## 74 Switching Power Supply Design

minimum,  $T_{\text{on}}$  will not have to be greater than  $0.8T/2$  to yield the specified value of  $V_o$ .

But  $V_o = V_1(2T_{\text{on}}/T)$ . Then

$$T_{\text{on}} = \frac{V_o T}{2V_1}$$

But  $N_s$  will be chosen so that  $T_{\text{on}}$  will be  $0.8T/2$  when  $V_{\text{dc}}$  and consequently,  $V_1$ , are at their minimum so that

$$\overline{T_{\text{on}}} = \frac{0.8T}{2} = \frac{V_o T}{2V_1} \quad \text{or} \quad \underline{V_1} = 1.25V_o$$

and

$$dI = \frac{(1.25V_o - V_o)(0.8T/2)}{L_o} = 2\underline{I_{\text{dc}}} \quad \text{and} \quad L_o = \frac{0.05V_o T}{\underline{I_{\text{dc}}}}$$

Then if the minimum current  $\underline{I_{\text{dc}}}$  is specified as one-tenth the nominal current  $I_{\text{on}}$  (the usual case),

$$L_o = \frac{0.5V_o T}{I_{\text{on}}} \quad (2.20)$$

where  $L_o$  is in henries

$V_o$  is in volts

$T$  is in seconds

$I_{\text{dc}}$  is minimum output current in amperes

$I_{\text{on}}$  is nominal output current in amperes

### 2.2.14.2 Output Capacitor Design

The output capacitor  $C_o$  is selected to meet the maximum output ripple voltage specification. In Section 1.3.7 it was shown that the output ripple is determined almost completely by the magnitude of the ESR (equivalent series resistance,  $R_o$ ) in the filter capacitor and not by the magnitude of the capacitor itself. The peak-to-peak ripple voltage  $V_r$  is very closely equal to

$$V_r = R_o dI \quad (2.21)$$

where  $dI$  is the selected peak-to-peak inductor ramp amplitude.

However, it was pointed out that (for aluminum electrolytic capacitors) the product  $R_o C_o$  has been observed to be relatively constant over a large range of capacitor magnitudes and voltage ratings.

## Chapter 2: Push-Pull and Forward Converter Topologies 75

For aluminum electrolytics, the product  $R_o C_o$  ranges between 50 and  $80 \times 10^{-6}$ . Then  $C_o$  is selected as

$$\begin{aligned} C_o &= \frac{80 \times 10^{-6}}{R_o} = \frac{80 \times 10^{-6}}{V_r/dI} \\ &= \frac{(80 \times 10^{-6})(dI)}{V_r} \end{aligned} \quad (2.22)$$

where  $C_o$  is in farads for  $dI$  in amperes (see Eq. 2.19) and  $V_r$  is in volts.

## 2.3 Forward Converter Topology

### 2.3.1 Basic Operation

A typical triple output forward converter topology is shown in Figure 2.10. This topology is often chosen for output powers under 200 W with DC supply voltages in the range of 60 to 200 V. Below 60 V, the primary input current becomes uncomfortably large at the higher power levels. Above about 250 V, the maximum voltage stress on the transistors becomes uncomfortably large.

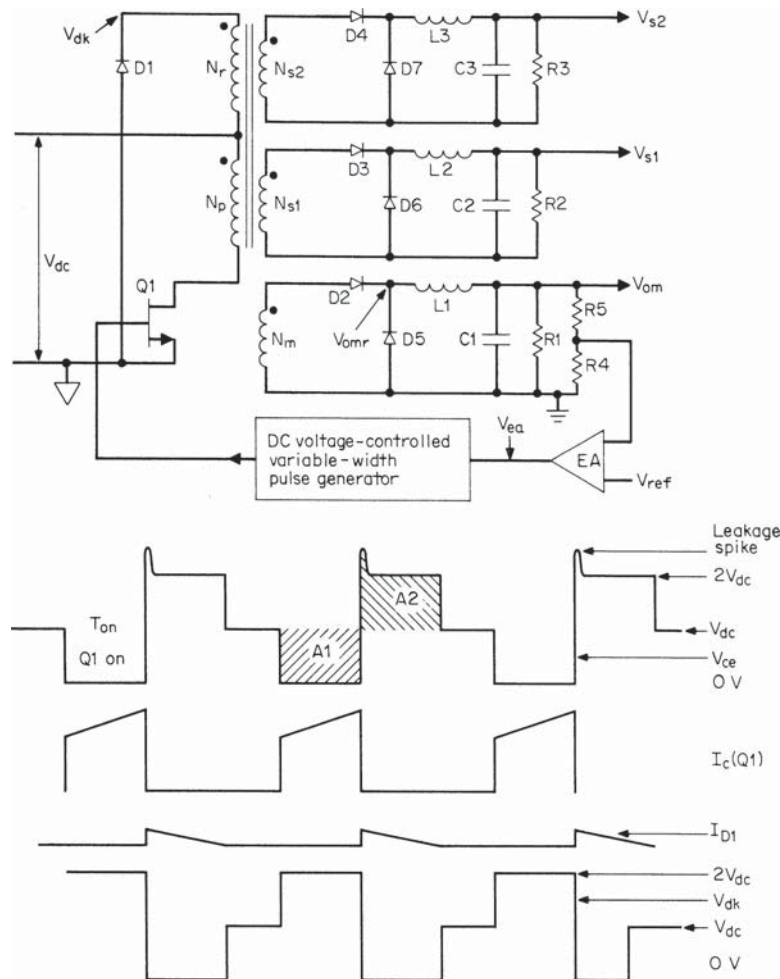
Further, it will be shown that above output powers of 200 W or so, the primary input current becomes too large even at the higher supply voltages. We will see this from the following mathematical analysis.

The topology is similar to the push-pull circuit of Figure 2.1, but does not suffer from the latter's major shortcoming of flux imbalance, since it has one rather than two transistors. Compared with the push-pull, at lower power it is more economical in cost and size.

In Figure 2.10 we see a master output  $V_{om}$  and two slaves,  $V_{s1}$  and  $V_{s2}$ . A negative-feedback loop is closed around the master, and controls the  $Q1$  "on" time so as to keep  $V_{om}$  constant against line and load changes. With an "on" time fixed by the master feedback loop, the slave outputs  $V_{s1}$  and  $V_{s2}$  are fully regulated against input voltage changes but only partly (about 5 to 8%) against load changes in themselves or in the master. The circuit works as follows.

If we compare the forward converter with the push-pull of Figure 2.1, we see that one of the transistors has been replaced by the diode  $D1$ . When  $Q1$  is turned "on," the start of the primary winding  $N_p$  (the dot end) and the start of all secondaries go positive. Current flows into the dot end of  $N_p$ . At the same time, all rectifier diodes  $D2$  to  $D4$  are forward-biased, and current flows out of the starts of all secondaries into the LC filters and the loads. Note that power flows into the loads when the power transistor  $Q1$  is turned "on," hence the term *forward converter*. Both the push-pull and buck regulators deliver power to

## 76 Switching Power Supply Design



**FIGURE 2.10** Forward converter topology and waveforms. In this example the feedback loop is closed around the chosen master output  $V_{om}$ , which is regulated against line and load changes. The two semiregulated slaves ( $V_{s1}$  and  $V_{s2}$ ) will be regulated against line changes only.

the loads when the power transistors are "on," so both are forward converters.

In contrast, the boost regulator, the polarity inverter (see Figures 1.10 and 1.14), and the flyback type (which will be discussed in a later chapter) store energy in an inductor or transformer primary when the power transistor is "on" and deliver it to the load when the transistor

## Chapter 2: Push-Pull and Forward Converter Topologies 77

turns “off.” Such energy storage topologies can operate in either the discontinuous or continuous mode. These topologies are fundamentally different from the forward converters and were discussed in Sections 1.4.2 and 1.4.3. They will be taken up again in Chapter 4, which covers the flyback topology.

Consider Figure 2.10: if transistor  $Q1$  has an “on” time of  $T_{on}$ , the voltage at the master rectifier cathode  $D5$  is at a high level for a period of  $T_{on}$ . Assuming a 1-V “on” voltage for  $Q1$  and a rectifier forward drop of  $V_{D2}$ , the high-level voltage  $V_{omr}$  is

$$V_{omr} = \left[ (V_{dc} - 1) \frac{N_m}{N_p} \right] - V_{D2} \quad (2.23)$$

The circuitry after the rectifier diode cathodes is exactly like that of the buck regulator of Figure 1.4. Diodes  $D5$  to  $D7$  act like the free-wheeling diode  $D1$  of that figure. When  $Q1$  turns “off,” the current established in the magnetizing inductance of  $T1$  while  $Q1$  was “on” (recall the equivalent circuit of a transformer as in Figure 2.7c) reverses the polarity of the voltage across  $N_p$ . Now all the starts (dot ends) of primary and secondary windings go negative. Without the “catch” action of diode  $D1$ , the dot end of  $N_r$  would go very far negative; since  $N_p$  and  $N_r$  usually have equal turns, the no-dot end of  $N_p$  would go sufficiently positive to avalanche  $Q1$  and destroy it.

However, with the catch action of diode  $D1$ , the dot end of  $N_r$  will be clamped at one diode drop below ground. If there were no leakage inductance in  $T1$  (recall again the equivalent circuit of a transformer as in Figure 2.7c), the voltage across  $N_p$  would equal that across  $N_r$ . Assuming that the 1-V forward drop across  $D1$  can be neglected, the voltage across  $N_r$  and  $N_p$  is  $V_{dc}$ , and the voltage at the no-dot end of  $N_p$  and at the  $Q1$  collector is then  $2V_{dc}$ .

We have seen previously that within one cycle, if a core has moved in one direction on its hysteresis loop, it must be restored to exactly its original position on the loop before it can be allowed to move in the same direction again in the next cycle. Otherwise, after many cycles, the core will “staircase” into saturation. If this is allowed to happen, the core will not be able to support the applied voltage, and the transistor will be destroyed.

Figure 2.10 shows that when  $Q1$  is “on” for a time  $T_{on}$ ,  $N_p$  is subjected to volt-second product  $V_{dc}T_{on}$  with its dot-end positive, that volt-second product is the area  $A1$  in Figure 2.10. By Faraday’s law (see Eq. 1.17), that volt-second product causes—say, a positive—flux change  $dB = (V_{dc}T_{on}/N_p A_e)10^{-8}$  gauss.

When  $Q1$  turns “off,” and the magnetizing inductance has reversed the polarity across  $N_p$  and kept its no-dot end at  $2V_{dc}$  long enough for the volt-second area product  $A2$  in Figure 2.10 to equal area  $A1$ , the core has been restored to its original position on the hysteresis loop,

## 78 Switching Power Supply Design

and the next cycle can safely start. We can see that the “reset volt-seconds” has equaled the “set volt-seconds.”

When  $Q1$  turns “off,” the dot ends of all secondaries go negative with respect to their no-dot ends. Current in all output inductors  $L1$  to  $L3$  will try to decrease. Since current in inductors cannot change instantaneously, the polarity across all inductors reverses in an attempt to maintain the current's constant. The input ends of the inductors try to go far negative, but are caught at one diode drop below output ground by free-wheeling diodes  $D5$  to  $D7$  (see Figure 2.10), and rectifier diodes  $D2$  to  $D4$  are reverse-biased. Inductor current now continues to flow in the same direction through the output end, returning through the load, partly through the filter capacitor, up through the free-wheeling diode and back into the inductor.

Voltage at the cathode of the main diode rectifier  $D2$  is then as shown in Figure 2.11b. It is high at a level of  $[(V_{dc} - 1)(N_m/N_p)] - V_{D2}$  for time  $T_{on}$ , and for a time  $T - T_{on}$  it is one free-wheeling diode ( $D5$ ) drop below ground. The  $LC$  filter averages this waveform, and assuming that the forward drop across  $D5$  equals that across  $D2$  ( $= V_d$ ), the DC output voltage at  $V_{om}$  is

$$V_{om} = \left[ \left( (V_{dc} - 1) \frac{N_m}{N_p} \right) - V_d \right] \frac{T_{on}}{T} \quad (2.24)$$

### 2.3.2 Design Relations: Output/Input Voltage, “On” Time, Turns Ratios

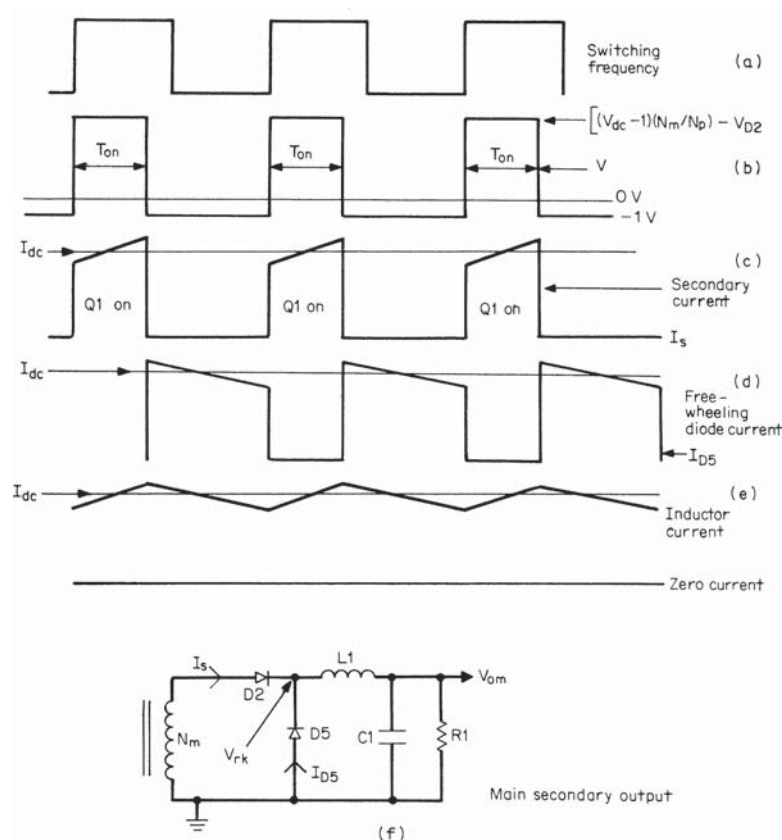
The negative-feedback loop senses a fraction of  $V_{om}$ , compares it with the reference voltage  $V_{ref}$ , and varies  $T_{on}$  so as to keep  $V_{om}$  constant for any changes in  $V_{dc}$  or load current.

From Eq. 2.24 it can be seen that as  $V_{dc}$  changes, the feedback loop keeps the output constant by keeping the product  $V_{dc}T_{on}$  constant. Thus maximum  $T_{on}(\overline{T_{on}})$  will occur at minimum specified  $V_{dc}(\underline{V_{dc}})$ , and Eq. 2.24 can be rewritten for minimum DC input voltage as

$$V_{om} = \left[ \left( (\underline{V_{dc}} - 1) \frac{N_m}{N_p} \right) - V_d \right] \frac{\overline{T_{on}}}{T} \quad (2.25)$$

In relation in Eq. 2.25, a number of design decisions must be made in the proper sequence. First, the minimum DC input voltage  $V_{dc}$  is specified. Then the maximum permitted “on” time  $T_{on}$ , which occurs at  $\underline{V_{dc}}$  (minimum  $V_{dc}$ ), will be set at 80% of a half period.

This margin is included to ensure (see Figure 2.10) that the area  $A2$  can equal  $A1$ . If the “on” time were permitted to go to a full half period,  $A2$  would just barely equal  $A1$  at the start of the next full cycle. Then any small increase in “on” time due to storage time changes with



**FIGURE 2.11** Critical secondary currents in forward converter. Each secondary has the characteristic ramp-on-a-step waveshape because of the fixed voltage across the output inductor during  $T_{on}$  and its constant inductance. Inductor current is the sum of the secondary plus the free-wheeling diode current. It ramps up and down about the DC output current. Primary current is the sum of all the ramp-on-a-step secondary currents, reflected by their turns ratios into the primary. Primary current is therefore also a ramp-on-a-step waveform.

temperature or production spreads would not permit  $A_2$  to equal  $A_1$ . The core would not be completely reset to its starting point on the hysteresis loop; it would drift up into saturation after a few cycles and destroy the transistor.

Next the number of primary turns  $N_p$  is established from Faraday's law (see Eq. 1.17) for  $V_{dc}$ , and a certain specified flux change  $\Delta B$  in the time  $T_{on}$ . Limits on that flux change are similar to those described

## 80 Switching Power Supply Design

for the push-pull topology in Section 1.5.9 and will also be discussed later.

Thus, in Eq. 2.25,  $\underline{V_{dc}}$ ,  $\overline{T_{on}}$ ,  $T$ , and  $V_d$  are specified, and  $N_p$  is calculated from Faraday's law. This fixes the number of main secondary turns  $N_m$  needed to achieve the required main output voltage  $V_{om}$ .

### 2.3.3 Slave Output Voltages

The slave output filters  $L2$ ,  $C2$  and  $L3$ ,  $C3$  average the width-modulated rectangular waveforms at their respective rectifier cathodes. The waveform upper levels are  $[(V_{dc} - 1)(N_{s1}/N_p)] - V_{d3}$  and  $[(V_{dc} - 1)(N_{s2}/N_p)] - V_{d4}$ , respectively. The low level voltages are one diode drop below ground. They are at the high level for the same maximum  $\overline{T_{on}}$  as is the main secondary, when the input DC input voltage is at the specified minimum  $\underline{V_{dc}}$ . Again assuming that the forward rectifier and free-wheeling diode drops equal  $V_d$ , the slave output voltages at low line  $\underline{V_{dc}}$  are

$$V_{s1} = \left[ \left( (\underline{V_{dc}} - 1) \frac{N_{s1}}{N_p} \right) - V_d \right] \frac{\overline{T_{on}}}{T} \quad (2.26)$$

$$V_{s2} = \left[ \left( (\underline{V_{dc}} - 1) \frac{N_{s2}}{N_p} \right) - V_d \right] \frac{\overline{T_{on}}}{T} \quad (2.27)$$

By regulating  $V_{om}$ , the feedback loop keeps  $V_{dc}T_{on}$  constant, but that same product appears in Eqs. 2.26 and 2.27, and hence the slave outputs remain constant as  $V_{dc}$  varies.

It can be seen from Eq. 2.24 and Figure 2.14 that the negative-feedback loop keeps the main output constant for either line or load changes by appropriately controlling  $T_{on}$  period, so that the sampled output is equal to the reference voltage  $V_{ref}$ . This is not so obvious for load changes, since load current does not appear directly in Eq. 2.24, but it does appear indirectly. Load changes will change the "on" voltage of Q1 (assumed as 1 V heretofore) and the forward drop in the rectifier diode. Although these changes are small, they will cause small changes in the output voltage that will be sensed and corrected by the error amplifier by making a small change in  $T_{on}$ .

Moreover, as can be seen in Eqs. 2.26 and 2.27, any change in  $T_{on}$  without a corresponding change in  $V_{dc}$  will cause the slave output voltages to change. The slave output voltages also change with changes in their own load currents. As those currents change, the rectifier forward drops also change, causing a change in the peak voltage at the input to the LC averaging filter. So slave output voltages will change the peak voltages to the averaging filters, with no corresponding change in  $T_{on}$ . Such changes in the slave output voltages as a result of load changes in the master and slave can be limited to within 5 to 8%.



## Chapter 2: Push-Pull and Forward Converter Topologies 81

As discussed in Section 2.2.4, neither master nor slave output inductors can be permitted to go discontinuous at their minimum load currents. This is ensured by choosing appropriately large output inductors, as will be described next.

The number of slave secondary turns  $N_{s1}$ ,  $N_{s2}$  are calculated from Eqs. 2.26 and 2.27, as all parameters there are either specified, or calculated from specified values. The parameters  $V_{dc}$ ,  $T$ , and  $V_d$  are all specified, and  $\overline{T_{on}}$  is set at  $0.8T/2$  as discussed earlier;  $N_p$  is calculated from Faraday's law (see Eq. 1.17) as described earlier.

### 2.3.4 Secondary Load, Free-Wheeling Diode, and Inductor Currents

Knowledge about the amplitudes and waveshapes of the various output currents is needed to select secondary and output inductor wire sizes and current ratings of the rectifiers and free-wheeling diodes.

As described for the buck regulator in Section 1.3.2, secondary current during the Q1 "on" time has the shape of an upward-sloping ramp sitting on a step (see Figure 2.11c) because of the constant voltage across the inductor during this time, with its input end positive with respect to the output end.

When Q1 turns "off," the input end of the inductor is negative with respect to the output end and inductor current ramps downward. The free-wheeling diode, at the instant of turn "off," picks up exactly the inductor current that had been flowing just prior to turn "off." That diode current then ramps downward (Figure 2.11d), as it is in series with the inductor. Inductor current is the sum of the secondary current when Q1 is "on" plus the free-wheeling diode current when Q1 is "off," and is shown in Figure 2.11e. Current at the center of the ramp in any of Figure 2.11c, 2.11d, or 2.11e is equal to the DC output current.

### 2.3.5 Relations Between Primary Current, Output Power, and Input Voltage

Assume an efficiency of 80% of the total output power from all secondaries to the DC power at the input voltage node. Then  $P_o = 0.8P_{in}$  or  $P_{in} = 1.25P_o$ . Now calculate  $P_{in}$  at minimum DC input voltage  $V_{dc}$ , which is  $V_{dc}$  times the average primary current at minimum DC input.

All secondary currents have the waveshape of a ramp sitting on a step because all secondaries have output inductors. These ramp-on-a-step waveforms have a width of  $0.8T/2$  at minimum DC input voltage. All these secondary currents are reflected into the primary by their turns ratios, and hence the primary current pulse is a single



## 82 Switching Power Supply Design

ramp-on-a-step waveform of width  $0.8T/2$ . There is only one such pulse per period (see Figure 2.10) as this is a single-transistor circuit. The duty cycle of this primary pulse is then  $(0.8T/2)/T$  or 0.4.

Like the push-pull topology, this ramp-on-a-step can be approximated by an equivalent flat-topped pulse  $I_{\text{pft}}$  of the same width and whose amplitude is that at the center of the ramp. The average value of this current is then  $0.4I_{\text{pft}}$ . Then

$$P_{\text{in}} = 1.25P_o = \frac{V_{\text{dc}}}{V_{\text{dc}}}(0.4I_{\text{pft}}) \quad \text{or} \quad I_{\text{pft}} = \frac{3.13P_o}{V_{\text{dc}}} \quad (2.28)$$

This is a valuable relation. It gives the equivalent peak flat-topped primary current pulse amplitude in terms of what is known at the outset—the minimum DC input voltage and the total output power. This permits an immediate selection of a transistor with adequate current rating and gain if it is a bipolar transistor, or with sufficiently low “on” resistance if it is a MOSFET type.

For a forward converter, Eq. 2.28 shows  $I_{\text{pft}}$  has twice the amplitude of that required in a push-pull topology (see Eq. 2.9) at the same output power and minimum DC input voltage.

This is obvious, because the push-pull has two pulses of current or power per period as compared with a single pulse in the forward converter. From Eq. 2.25, if the number of secondary turns in the forward converter is chosen large enough, then the maximum “on” time at minimum DC input voltage will not need to be greater than 80% of a half period. Then, as seen in Figure 2.10, the area  $A_2$  can always equal  $A_1$  before the start of the next period. The core is then always reset to the same point on its hysteresis loop within one cycle and can never walk up into saturation.

The penalty paid for this guarantee that flux walking cannot occur in the forward converter is that the primary peak current is twice that for a push-pull at the same output power. Despite all the precautions described in Section 2.2.8, however, there is never complete certainty in the push-pull that flux imbalance will not occur under unusual dynamic load or line conditions.

### 2.3.6 Maximum Off-Voltage Stress in Power Transistor

In the forward converter, with the number of turns on the reset winding  $N_r$  equal to that on the power winding  $N_p$ , maximum off-voltage stress on the power transistor is twice the maximum DC input voltage plus a leakage inductance spike. These spikes and their origin and minimization have been discussed in Section 2.2.11. Conservative design, even with all precautions to minimize leakage spikes, should

## Chapter 2: Push-Pull and Forward Converter Topologies 83

assume they may be 30% above twice the maximum DC input voltage. Maximum off-voltage stress is then the same as in the push-pull and is

$$V_{ms} = 1.3(2\overline{V_{dc}}) \quad (2.29)$$

### 2.3.7 Practical Input Voltage/ Output Power Limits

It was stated at the outset in Section 2.3.1 that the practical maximum output power limit for a forward converter whose maximum DC input voltage is under 60 V is 150 to 200 W. This is so because the peak primary current as calculated from Eq. 2.28 becomes excessive, as there is only a single pulse per period as compared with two in the push-pull topology.

Thus consider a 200-W forward converter for the telephone industry in which the specified minimum and maximum input voltages are 38 and 60 V, respectively. Peak primary current from Eq. 2.28 is  $I_{pft} = 3.13P_o/\overline{V_{dc}} = 3.13(200)/38 = 16.5$  A, and from Eq. 2.29, maximum off-voltage stress is  $\overline{V_{ms}} = 2.6\overline{V_{dc}} = 2.6 \times 60 = 156$  V.

To provide a safety margin, a device with at least a 200-V rating would be used to provide protection against input voltage transients that could drive the DC input above the maximum steady-state value of 60 V.

Transistors with 200-V, 16-A ratings are available, but they all have drawbacks as discussed in Section 2.2.13. Bipolar transistors are slow, and MOSFETs are easily fast enough but expensive. For such a 200-W application, a push-pull version guaranteed to be free from flux imbalance would be preferable; with two pulses of current per period, peak current would be only 8 A. With the resulting lower peak current noise spikes on the ground buses, the radio-frequency interference (RFI) would be considerably lower—a very important consideration for a telephone industry power supply. Such a flux imbalance-free topology is *current mode*, which is discussed later.

The forward converter topology, like the push-pull (discussed in Section 2.2.13), has the same difficulty in coping with maximum voltage stress in an offline converter where the nominal AC input voltage is  $120 \pm 10\%$ . At high line, the rectified DC input is  $1.1 \times 120 \times 1.41 = 186$  V minus 2 V for the rectifier diode drops or 184 V. From Eq. 2.29, the maximum voltage stress on the transistor in the “off” state is  $\overline{V_{ms}} = 2.6 \times 184 = 478$  V.

At minimum AC input voltage, the rectified DC output is  $\overline{V_{dc}} = (0.9 \times 120 \times 1.41) - 2 = 150$  V, and from Eq. 2.28, the peak primary current is  $I_{pft} = 3.13 \times 22/150 = 4.17$  A.

## 84 Switching Power Supply Design

Thus, for a 200-W offline forward converter the problem is more the 478-V maximum voltage stress than the 4.17-A peak primary current stress. As was seen in Section 2.2.13, when a 15% input transient is taken into account, the peak off-voltage stress is 550 V. With a bipolar transistor operating under  $V_{ceV}$  conditions (reverse input bias of  $-1$  to  $-5$  V at the instant of turn “off”), a voltage stress of even 550 V is not a serious restriction. Many devices have 650- to 850-V  $V_{ceV}$  ratings and high gain, low “on” drop, and high speed at 4.17 A. But, as discussed in Section 2.2.13, there are preferable topologies, discussed next, that subject the off transistor to only  $V_{dc}$  and not twice  $V_{dc}$ .

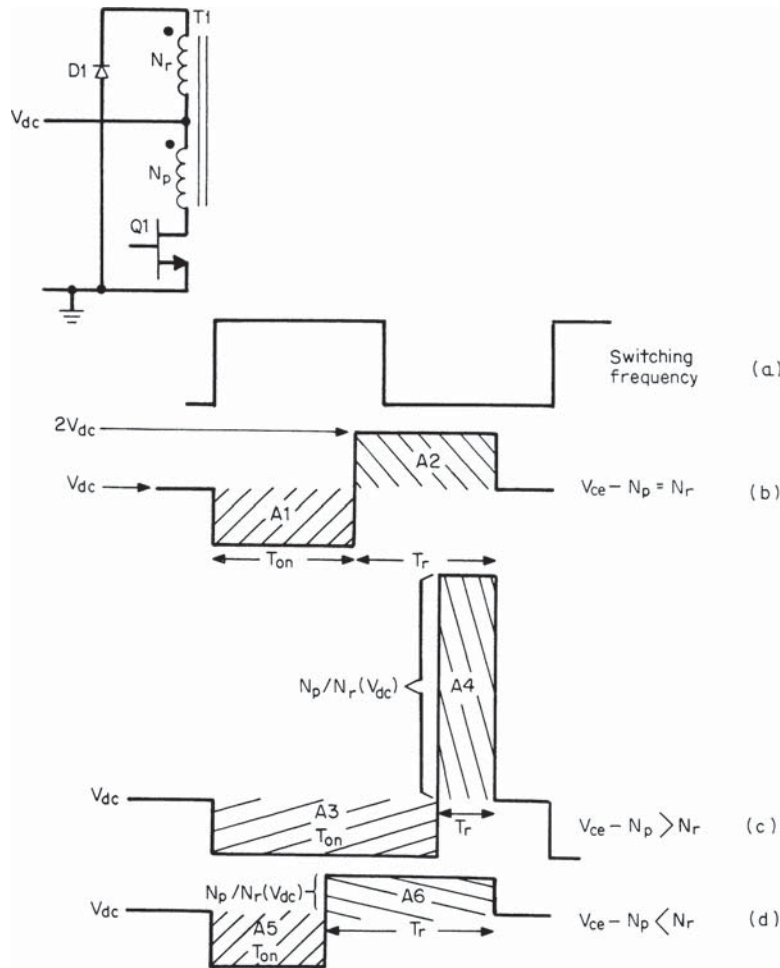
### 2.3.8 Forward Converter With Unequal Power and Reset Winding Turns

Heretofore it has been assumed that the numbers of turns on the power winding  $N_p$  and the reset winding  $N_r$  are equal. Some advantages result if  $N_r$  is made less or greater than  $N_p$ .

The number of primary power turns  $N_p$  is always chosen by Faraday’s law and will be discussed in Section 2.3.10.2. If  $N_r$  is chosen less than  $N_p$ , the peak current required for a given output power is less than that calculated from Eq. 2.28, but the maximum Q1 off-voltage stress is greater than that calculated from Eq. 2.29. If  $N_r$  is chosen larger than  $N_p$ , the maximum Q1 off-voltage stress is less than that calculated from Eq. 2.29, but the peak primary current for a given output power is greater than that calculated from Eq. 2.28. This can be seen from Figure 2.12 as follows. When Q1 turns “off,” polarities across  $N_p$  and  $N_r$  reverse; the dot end of  $N_r$  goes negative and is caught at ground by catch diode D1. Transformer T1 is now an autotransformer. There is a voltage  $V_{dc}$  across  $N_r$  and hence a voltage  $N_p/N_r(V_{dc})$  across  $N_p$ . The core is set by the volt-second product by  $V_{dc}T_{on}$  during the “on” time and must be reset to its original place on the hysteresis loop by an equal volt-second product. That reset volt-second product is  $N_p/N_r(V_{dc})T_r$ .

When  $N_r$  equals  $N_p$ , the reset voltage equals the set voltage, and the reset time is equal to the set time (area A1 = area A2) as seen in Figure 2.12b. For  $N_r = N_p$ , the maximum Q1 “on” time that occurs at minimum DC input voltage is chosen as  $0.8T/2$  to ensure that the core is reset before the start of the next period;  $T_{on} + T_r$  is then  $0.8T$ .

Now if  $N_r$  is less than  $N_p$ , the resetting voltage is larger than  $V_{dc}$  and consequently  $T_r$  can be smaller (area A3 = area A4) as shown in Figure 2.12c. With a shorter  $T_r$ ,  $T_{on}$  can be longer than  $0.8T/2$ , and  $T_{on} + T_r$  can still be  $0.8T$  so that the core is reset before the start of the next period. With a longer  $T_{on}$ , the peak current is smaller for the same average current and the same average output power. Thus in Figure 2.12c, a



**FIGURE 2.12** Forward converter—collector-to-emitter voltages for three  $N_p$  to  $N_r$  ratios. Note in all cases that reset volt-second product equals set volt-second product. (a) Switching frequency, (b)  $N_p = N_r$ , (c)  $N_p > N_r$ , (d)  $N_p < N_r$ .

smaller peak current stress has been traded for a longer voltage stress than in Figure 2.12b.

With  $N_r$  greater than  $N_p$ , the reset voltage is less than  $V_{dc}$ . Then if  $T_{on} + T_r$  is still to equal  $0.8T$ , and the reset volt-seconds is to equal the set volt-seconds (area  $A_5 = \text{area } A_6$  in Figure 2.12d),  $T_r$  must be longer and  $T_{on}$  must be shorter than  $0.8T/2$ , as the reset voltage is

## 86 Switching Power Supply Design

less than the set voltage. With  $T_{\text{on}}$  less than  $0.8T/2$ , the peak current must be higher for the same average current. Thus, in Figure 2.12*d*, a lesser voltage stress has been achieved at the cost of a higher peak current for the same output power as in Figure 2.12*b*. This can be seen quantitatively as

$$\text{Set } T_{\text{on}} + T_r = 0.8T; \quad \text{reset voltage} = V_r = \frac{N_p}{N_r} V_{\text{dc}} \quad (2.30)$$

For “on” volt-seconds equal to reset volt-seconds,

$$V_{\text{dc}} T_{\text{on}} = \frac{N_p}{N_r} V_{\text{dc}} T_r \quad (2.31)$$

Combining Eqs. 2.30 and 2.31,

$$\overline{T_{\text{on}}} = \frac{0.8T}{1 + N_r/N_p} \quad (2.32)$$

For 80% efficiency  $P_{\text{in}} = 1.25P_o$  and  $P_{\text{in}}$  at  $\underline{V_{\text{dc}}} = V_{\text{dc}}(I_{\text{av}}) = \underline{V_{\text{dc}}} I_{\text{pft}}(\overline{T_{\text{on}}})/T$  or  $I_{\text{pft}} = 1.25(P_o/\underline{V_{\text{dc}}})(T/T_{\text{on}})$ . Then from Eq. 2.32

$$I_{\text{pft}} = 1.56 \left( \frac{P_o}{\underline{V_{\text{dc}}}} \right) (1 + N_r/N_p) \quad (2.33)$$

and the maximum Q1 off-voltage stress  $\overline{V_{\text{ms}}}$ —exclusive of the leakage spike—is the maximum DC input voltage  $V_{\text{dc}}$  plus the reset voltage (voltage across  $N_p$  when the dot end of  $N_r$  is at ground). Thus

$$\overline{V_{\text{ms}}} = \overline{V_{\text{dc}}} + \frac{N_p}{N_r}(\overline{V_{\text{dc}}}) = \overline{V_{\text{dc}}}(1 + N_p/N_r) \quad (2.34)$$

Values of  $I_{\text{pft}}$  and  $V_{\text{ms}}$  calculated from Eqs. 2.33 and 2.34 are

$N_r/N_p$	$I_{\text{pft}}$ (from Eq. 2.33)	$V_{\text{ms}}$ (from Eq. 2.34)
0.6	$2.50(P_o/\underline{V_{\text{dc}}})$	$2.67 \overline{V_{\text{dc}}} + \text{leakage spike}$
0.8	$2.81(P_o/\underline{V_{\text{dc}}})$	$2.25 \underline{V_{\text{dc}}} + \text{''''}$
1.0	$3.12(P_o/\underline{V_{\text{dc}}})$	$2.00 \underline{V_{\text{dc}}} + \text{''''}$
1.2	$3.43(P_o/\underline{V_{\text{dc}}})$	$1.83 \underline{V_{\text{dc}}} + \text{''''}$
1.4	$3.74(P_o/\underline{V_{\text{dc}}})$	$1.71 \underline{V_{\text{dc}}} + \text{''''}$
1.6	$4.06(P_o/\underline{V_{\text{dc}}})$	$1.62 \underline{V_{\text{dc}}} + \text{''''}$

### 2.3.9 Forward Converter Magnetics

#### 2.3.9.1 First-Quadrant Operation Only

The transformer core in the forward converter operates in the first quadrant of the hysteresis loop only. This can be seen in Figure 2.10.

## Chapter 2: Push-Pull and Forward Converter Topologies 87

When  $Q1$  is “on,” the dot end of  $T1$  is positive with respect to the no-dot end, and the core is driven, say, in a positive direction on the hysteresis loop, and the magnetizing current ramps up linearly in the magnetizing inductance.

When  $Q1$  turns “off,” stored current in the magnetizing inductance reverses the polarity of voltages on all windings. The dot end of  $N_r$  goes negative until it is caught one diode drop below ground by catch diode  $D1$ . Now the magnetizing current that is stored in the magnetic core continues to flow. It simply transfers from  $N_p$ , where it had ramped upward during the  $Q1$  “on” time, into  $N_r$  where it ramps back to zero during the “off” time. It flows out of the no-dot end of  $N_r$  into the positive end of the supply voltage  $V_{dc}$ , out of the negative end of  $V_{dc}$ , through  $D1$ , and back into  $N_r$ .

Since the dot end of  $N_r$  is positive with respect to its no-dot end during the  $Q1$  “off” time, the magnetizing current  $I_d$  ramps linearly downward, as can be seen in Figure 2.10. When it has ramped down to zero (at the end of area  $A2$  in Figure 2.10), there is no longer any stored energy in the magnetizing inductance and nothing to hold the dot end of  $N_r$  below the  $D1$  cathode. The voltage at the dot end of  $N_r$  starts rising toward that at the  $D1$  cathode. The voltage at the dot end of  $N_r$  starts rising toward  $V_{dc}$ , and that at the no-dot end of  $N_p$  ( $Q1$  collector) starts falling from  $2V_{dc}$  back down toward  $V_{dc}$ .

Thus operation on the hysteresis loop is centered about half the peak magnetizing current ( $V_{dc}T_{on}/2L_m$ ). Nothing ever reverses the direction of the magnetizing current—it simply builds up linearly to a peak and relaxes back down linearly to zero.

This first-quadrant operation has some favorable and some unfavorable consequences. First, compared with a push-pull circuit, it halves the available output power from a given core. This can be seen from Faraday’s law (see Eq. 1.17), which fixes the number of turns on the primary.

By solving Faraday’s law for the number of primary turns, we get  $N_p = E dt/A_e dB \times 10^{-8}$ . If  $dB$  in the forward converter is limited to an excursion from zero to some  $B_{max}$ , instead of from  $-B_{max}$  to  $+B_{max}$  as in a push-pull topology, the number of primary turns for the forward converter will be twice that in each half primary of a push-pull operating from the same  $V_{dc}$ . Although the push-pull has two half primaries, each of which must support the same volt-second product as the forward converter primary, the push-pull provides two power pulses per period as compared with one for the forward converter. The end result is that a core used in a forward converter can process only half the output power available from the same core in a push-pull configuration.

However, the push-pull core at twice the output power will run somewhat warmer, as its flux excursion is twice that of the forward

## 88 Switching Power Supply Design

converter. Since core losses are proportional to the area of the hysteresis loop traversed, the push-pull core losses are twice that of the forward converter.

Yet total copper losses in both half primaries of a push-pull are no greater than that of a forward converter of half the output power, because the rms current in each push-pull half primary is equal to that in the forward converter primary. Since the number of turns in each push-pull half primary is half that of the forward converter primary of half the output power, they also have half the resistance. Thus total copper loss in a forward converter is equal to the total loss of the two half primaries in a push-pull of twice the output power.

### 2.3.9.2 Core Gapping in a Forward Converter

In Figure 2.3, we see the hysteresis loop of a ferrite core with no air gap. We see that at zero magnetizing force (0 Oe) there is a residual magnetic flux density of about  $\pm 1000$  G. This residual flux is referred to as *remanence*.

In a forward converter, if the core started at 0 Oe and hence at 1000 G, the maximum flux change in  $dB$  possible before the core is driven up into the curved part of the hysteresis loop is about 1000 G. It is desirable to stay off the curved part of the hysteresis loop, and hence the forward converter core with no air gap is restricted to a maximum  $dB$  of 1000 G. As shown earlier, the number of primary turns is inversely proportional to  $dB$ . Such a relatively small  $dB$  requires a relatively large number of primary turns. A large number of primary turns requires small wire size and hence decreases the current and power available from the transformer.

By introducing an air gap in the core, the hysteresis loop is tilted as shown in Figure 2.5, and magnetic remanence is reduced significantly. The hysteresis loop tilts over but still crosses the  $H$  (*coercive force*) axis with zero flux density at the same point. Coercive force for ferrites is seen to be about 0.2 Oe in Figure 2.3. An air gap of 2 to 4 mils will reduce remanence to about 200 G for most cores used at 200 to 500 W of output power. With remanence of 200 G, the  $dB$  before the core enters the curved part of the hysteresis loop is now about 1800 G, and fewer turns are permissible.

However, a penalty is paid in introducing an air gap. Figure 2.5 shows the slope of the hysteresis loop tilted over. The slope is  $dB/dH$  or core permeability, which has been decreased by adding the gap. Decreasing permeability decreases magnetizing inductance and increases magnetizing current ( $I_m = V_{dc}T_{on}/L_m$ ). Magnetizing current contributes no output power to the load; it simply moves the operating point of the core around the hysteresis loop and contributes significant copper loss if it exceeds 10% of the primary load current.



### 2.3.9.3 Magnetizing Inductance with Gapped Core

Magnetizing inductance with a gapped core can be calculated as follows. Voltage across the magnetizing inductance is  $L_m dI_m/dt$  and from Faraday's law:

$$V_{dc} = \frac{L_m dI_m}{dt} = \frac{N_p A_e dB}{dt} 10^{-8} \quad \text{or} \quad L_m = \frac{N_p A_e dB}{dI_m} 10^{-8} \quad (2.35)$$

where  $L_m$  = magnetizing inductance, H

$N_p$  = number of primary turns

$A_e$  = core area,  $\text{cm}^2$

$dB$  = core flux change, G

$dI_m$  = change in magnetizing current, A

A fundamental law in magnetics is Ampere's law:

$$\int H \cdot dl = 0.4\pi NI$$

This states that if a line is drawn encircling a number of ampere turns  $NI$ , the dot product  $H \cdot dl$  along that line is equal to  $0.4\pi NI$ . If the line is taken through the core parallel to the magnetic flux lines and across the gap, since  $H$  is uniform at a value  $H_i$  within the core and uniform at a value  $H_a$  within the gap, then

$$H_i l_i + H_a l_a = 0.4\pi NI_m \quad (2.36)$$

where  $H_i$  = magnetic field intensity in iron (ferrite), Oe

$l_i$  = length of iron path, cm

$H_a$  = magnetic field intensity in air gap, Oe

$l_a$  = length of air gap, cm

$I_m$  = magnetizing current, A

However,  $H_i = B_i/u$ , where  $B_i$  is the magnetic flux density in iron and  $u$  is the iron permeability;  $H_a = B_a$  as the permeability of air is 1; and  $B_a = B_i$  (flux density in iron = flux density in air) if fringing flux around the air gap is ignored. Then Eq. 2.36 can be written as

$$\frac{B_i}{u} l_i + B_i l_a = 0.4\pi N_p I_m \quad \text{or} \quad B_i = \frac{0.4\pi N I_m}{l_a + l_i/u} \quad (2.37)$$

Then  $dB/dI_m = 0.4\pi N/(l_a + l_i/u)$ , and substituting this into Eq. 2.35:

$$L_m = \frac{0.4\pi (N_p)^2 A_e \times 10^{-9}}{l_a + l_i/u} \quad (2.38)$$



## 90 Switching Power Supply Design

Thus, introducing an air gap of length  $l_a$  to a core of iron path length  $l_i$  reduces the magnetizing inductance in the ratio of

$$\frac{L_m \text{ (with gap)}}{L_m \text{ (without gap)}} = \frac{l_i/u}{l_a + l_i/u} \quad (2.39)$$

It is instructive to consider a specific example. Take an international standard core such as the Ferroxcube 783E608-3C8. It has a magnetic path length of 9.7 cm and an effective permeability of 2300. Then if a 4-mil (= 0.0102-cm) gap were introduced into the magnetic path, from Eq. 2.39:

$$\begin{aligned} L_m \text{ (with gap)} &= \frac{9.7/2300}{0.0102 + 9.7/2300} L_m \text{ (without gap)} \\ &= 0.29 L_m \text{ (without gap)} \end{aligned}$$

A useful way of looking at a gapped core is to examine the denominator in Eq. 2.38. In most cases,  $u$  is so high that the term  $l_i/u$  is small compared with the air gap  $l_a$ , and the inductance is determined primarily by the length of the air gap.

### 2.3.10 Power Transformer Design Relations

#### 2.3.10.1 Core Selection

As discussed in Section 2.2.9.1 on core selection for a push-pull transformer, the amount of power available from a core for a forward converter transformer is related to the same parameters—peak flux density, core iron and window areas, frequency, and coil current density in circular mils per rms ampere.

In Chapter 7, an equation will be derived giving the amount of available output power as a function of these parameters. This equation will be converted to a chart that permits selection of core size and operating frequency at a glance.

For the present, it is assumed that a core has been selected and that its iron and window areas are known.

#### 2.3.10.2 Primary Turns Calculation

The number of primary turns is calculated from Faraday's law as given in Eq. 2.7. From Section 2.3.9.2, we see that in the forward converter with a gapped core, flux density moves from about 200 G to some higher value  $B_{\max}$ .

In the push-pull topology as discussed in Section 2.2.9.4, this peak value will be set at 1600 G (for ferrites at low frequencies, where core losses are not a limiting factor). This avoids the problem of a much larger and more dangerous flux swing due to rapid changes in DC

## Chapter 2: Push-Pull and Forward Converter Topologies 91

input voltage or load currents. Such rapid changes are not immediately compensated because the limited error-amplifier bandwidth can't correct the power transistor "on" time fast enough.

During this error-amplifier delay, the peak flux density can exceed the calculated normal steady-state value for a number of cycles. This can be tolerated if the normal peak flux density in the absence of a line or load transient is set to the low value of 1600 G. As discussed earlier, the excursion from approximately zero to 1600 G will take place in 80% of a half period to ensure that the core can be reset before the start of the next period (see Figure 2.12b).

Thus, the number of primary turns is set by Faraday's law at

$$N_p = \frac{(V_{dc} - 1)(0.8T/2) \times 10^{+8}}{A_e dB} \quad (2.40)$$

where  $V_{dc}$  = minimum DC input, V

$T$  = operating period, s

$A_e$  = iron area, cm<sup>2</sup>

$dB$  = change in flux density, G

### 2.3.10.3 Secondary Turns Calculation

Secondary turns are calculated from Eqs. 2.25 to 2.27. In those relations, all values except the secondary turns are specified or already calculated. Thus (see Figure 2.10):

$V_{dc}$  = minimum DC input, V

$T_{on}$  = maximum "on" time, s (= 0.8T/2)

$N_m, N_{s1}, N_{s2}$  = numbers of main and slave turns

$N_p$  = number of primary turns

$V_d$  = rectifier forward drop

If the main output produces 5 V at high current as is often the case, a Schottky diode with forward drop of about 0.5 V is typically used. The slaves usually have higher output voltages that require the use of fast-recovery diodes with higher reverse-voltage ratings. Such diodes have forward drops of about 1.0 V over a large range of current.

### 2.3.10.4 Primary rms Current and Wire Size Selection

Primary equivalent flat-topped current is given by Eq. 2.28. That current flows for a maximum of 80% of a half period per period, so its maximum duty cycle is 0.4. Recalling that the rms value of a flat-topped

## 92 Switching Power Supply Design

pulse of amplitude  $I_p$  is  $I_{\text{rms}} = I_p \sqrt{T_{\text{on}}/T}$ , the rms primary current is

$$\begin{aligned} I_{\text{rms(primary)}} &= \frac{3.12 P_o}{V_{\text{dc}}} \sqrt{0.4} \\ &= \frac{1.97 P_o}{V_{\text{dc}}} \end{aligned} \quad (2.41)$$

If the wire size is chosen on the basis of 500 circular mils per rms ampere, the required number of circular mils is

$$\begin{aligned} \text{Circular mils needed} &= \frac{500 \times 1.97 P_o}{V_{\text{dc}}} \\ &= \frac{985 P_o}{V_{\text{dc}}} \end{aligned} \quad (2.42)$$

### 2.3.10.5 Secondary rms Current and Wire Size Selection

It is seen in Figure 2.11 that the secondary current has the characteristic shape of a ramp on a step. The pulse amplitude at the center of the ramp is equal to the average DC output current. Thus, the equivalent flat-topped secondary current pulse at  $V_{\text{dc}}$  (when its width is a maximum) has amplitude  $I_{\text{dc}}$ , width  $0.8T/2$ , and duty cycle  $(0.8T/2)/T$  or 0.4. Then

$$\begin{aligned} I_{\text{rms(secondary)}} &= I_{\text{dc}} \sqrt{0.4} \\ &= 0.632 I_{\text{dc}} \end{aligned} \quad (2.43)$$

and at 500 circular mils per rms ampere, the required number of circular mils for each secondary is

$$\begin{aligned} \text{Circular mils needed} &= 500 \times 0.632 I_{\text{dc}} \\ &= 316 I_{\text{dc}} \end{aligned} \quad (2.44)$$

### 2.3.10.6 Reset Winding rms Current and Wire Size Selection

The reset winding carries only magnetizing current, as can be seen by the dots in Figure 2.10. When  $Q1$  is "on," diode  $D1$  is reverse-biased, and no current flows in the reset winding. But magnetizing current builds up linearly in the power winding  $N_p$ . When  $Q1$  turns "off," that magnetizing current must continue to flow. When  $Q1$  current ceases, the current in the magnetizing inductance reverses all winding voltage polarities. When  $D1$  clamps the dot end of  $N_r$  to ground, the magnetizing current transfers from  $N_p$  to  $N_r$  and continues flowing through the DC input voltage source  $V_{\text{dc}}$ , through  $D1$ , and back into  $N_r$ . Since the no-dot end of  $N_r$  is positive with respect to the dot end, the magnetizing current ramps downward to zero as seen in Figure 2.10.

## Chapter 2: Push-Pull and Forward Converter Topologies 93

The waveshape of this  $N_r$  current is the same as that of the magnetizing current that ramped upward when  $Q_1$  was “on,” but it is reversed from left to right. Thus the peak of this triangle of current is  $I_{p(\text{magnetizing})} = \overline{V_{dc} T_{on}} / L_{mg}$ , where  $L_{mg}$  is the magnetizing inductance with an air gap as calculated from Eq. 2.39. The inductance without the gap is calculated from the ferrite catalog value of  $A_l$ , the inductance per 1000 turns. Since inductance is proportional to the square of the number of turns, inductance for  $n$  turns is  $L_n = A_l(n/1000)^2$ . The duration of this current triangle is  $0.8T/2$  (the time required for the core to reset), and it comes at a duty cycle of 0.4.

It is known that the rms value of a repeating triangle waveform (no spacing between successive triangles) of peak amplitude  $I_p$  is  $I_{rms} = I_p \sqrt{3}$ . But this triangle comes at a duty cycle of 0.4, and hence its rms value is

$$\begin{aligned} I_{rms} &= \frac{\overline{V_{dc} T_{on}}}{L_{mg}} \frac{\sqrt{0.4}}{\sqrt{3}} \\ &= 0.365 \frac{\overline{V_{dc} T_{on}}}{L_{mg}} \end{aligned}$$

and at 500 circular mils per rms ampere, the required number of circular mils for the reset winding is

$$\text{Circular mils required} = 500 \times 0.365 \frac{\overline{V_{dc} T_{on}}}{L_{mg}} \quad (2.45)$$

Most frequently, the magnetizing current is so small that the reset winding wire can be No. 30 AWG or smaller.

### 2.3.11 Output Filter Design Relations

The output filters  $L1C1$ ,  $L2C2$ , and  $L3C3$  average the voltage waveform at the rectifier cathodes. The inductor is selected to operate in continuous mode (see Section 1.3.6) at the minimum DC output current. The capacitor is selected to yield a specified minimum output ripple voltage.

#### 2.3.11.1 Output Inductor Design

Recall from Section 1.3.6 that discontinuous mode condition occurs when the inductor current ramp drops to zero (see Figure 2.10). Since the DC output current is the value at the center of the ramp, discontinuous mode occurs at a minimum current  $I_{dc}$  equal to half the ramp amplitude  $dI$  as can be seen in Figure 2.10.

## 94 Switching Power Supply Design

Now referring to Figure 2.11,

$$dI = 2I_{dc} = \frac{(V_{rk} - V_o)\overline{T_{on}}}{L1} \quad \text{or} \quad L1 = \frac{(V_{rk} - V_o)\overline{T_{on}}}{2I_{dc}}$$

But  $V_o = V_{rk}\overline{T_{on}}/T$ . Then

$$\begin{aligned} L1 &= \left( \frac{V_o T}{\overline{T_{on}}} - V_o \right) \frac{\overline{T_{on}}}{2I_{dc}} \\ &= \frac{V_o(T/\overline{T_{on}} - 1)/\overline{T_{on}}}{2I_{dc}} \end{aligned}$$

But  $\overline{T_{on}} = 0.8T/2$ . Then

$$L1 = \frac{0.3V_o T}{I_{dc}} \quad (2.46)$$

and if the minimum DC current  $I_{dc}$  is one-tenth the nominal output current  $I_{on}$ , then

$$L1 = \frac{3V_o T}{I_{on}} \quad (2.47)$$

### 2.3.11.2 Output Capacitor Design

It was seen in Section 1.3.7 that the output ripple is almost completely determined by the equivalent series resistance  $R_o$  of the filter capacitor. The peak-to-peak ripple amplitude is  $V_{or} = R_o dI$ , where  $dI$  is the peak-to-peak ripple current amplitude chosen by the selection of the ripple inductor as discussed earlier. Assuming that the average value of  $R_o C_o$  for aluminum electrolytic capacitors over a large range of voltage and capacitance ratings is given by  $R_o C_o = 65 \times 10^{-6}$  as in Section 1.3.7, then

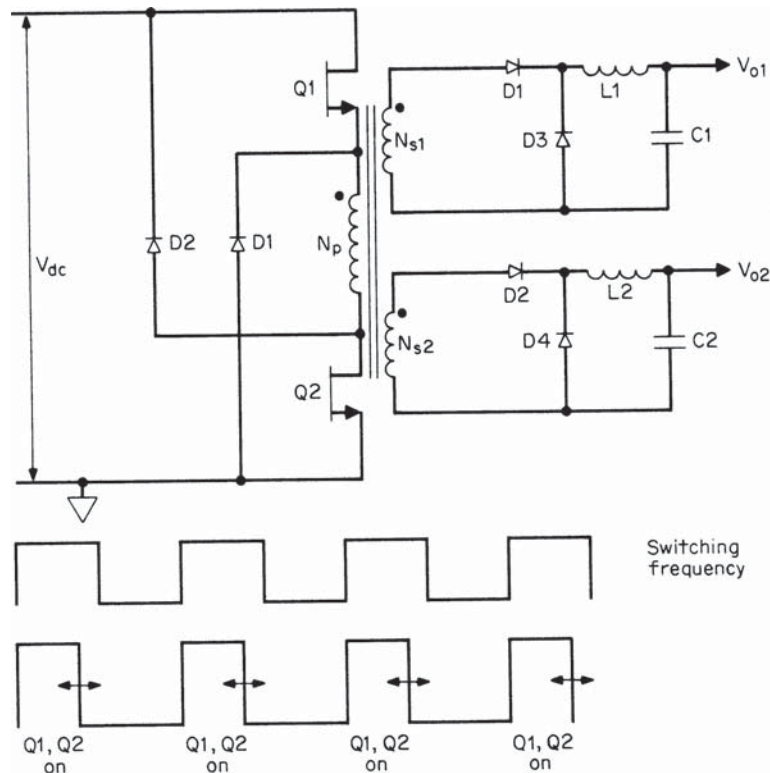
$$\begin{aligned} C_o &= 65 \times 10^{-6} / R_o \\ &= 65 \times 10^{-6} \frac{dI}{V_{or}} \end{aligned} \quad (2.48)$$

where  $dI$  is in amperes and  $V_{or}$  is in volts for  $C_o$  in farads.

## 2.4 Double-Ended Forward Converter Topology

### 2.4.1 Basic Operation

Double-ended forward converter topology is shown in Figure 2.13. Although it has two transistors rather than one compared with the single-ended forward converter of Figure 2.10, it has a very significant



**FIGURE 2.13** Double-ended forward converter. Transistors  $Q1$  and  $Q2$  are turned on and off simultaneously. Diodes  $D1$  and  $D2$  keep the maximum off-voltage stress on  $Q1$ ,  $Q2$  at a maximum of  $V_{dc}$  as contrasted with  $2V_{dc}$  plus a leakage spike for the single-ended forward converter of Figure 2.10.

advantage. In the “off” state, both transistors are subjected to only the DC input voltage rather than twice that, as in the single-ended converter. Further, at turn “off,” there is no leakage inductance spike.

It was pointed out in Section 2.3.7 that the off-voltage stress in the single-ended forward converter operating from a nominal 120-V AC line can be as high as 550 V when there is a 15% transient above a 10% steady-state high line and a 30% leakage spike.

Although a number of bipolar transistors have  $V_{ceV}$  ratings up to 650 and even 850 V that can take that stress, it is far more reliable to use a double-ended forward converter with half the off-voltage stress. Reliability is of overriding importance in a power supply design, and in any weighing of reliability versus initial cost, the best and—in the long run—least expensive choice is reliability.

## 96 Switching Power Supply Design

Further, for power supplies to be used in the European market where the AC voltage is 220 V (rectified DC voltage is nominally about 308 V), the single-ended forward converter is not usable at all because of the excessive voltage stress on the off transistor (see Eq. 2.29). The double-ended forward converter, the half bridge, and the full bridge (to be discussed in Chapter 3) are the only choices for equipment to be used in the European market.

The double-ended forward converter works as follows. In Figure 2.13,  $Q1$  and  $Q2$  are in series with the transformer primary. These transistors are turned on and off simultaneously. When they are “on,” all primary and secondary dot ends are positive, and power is delivered to the loads. When they turn “off,” current stored in the  $T1$  magnetizing inductance reverses the voltage polarity of all windings. The negative-going dot end of  $N_p$  is caught at ground by diode  $D1$ , and the positive-going no-dot end of  $N_p$  is caught at  $V_{dc}$  by diode  $D2$ .

Thus the emitter of  $Q1$  can never be more than  $V_{dc}$  below its collector, and the collector of  $Q2$  can never be more than  $V_{dc}$  above its emitter. Leakage inductance spikes are clamped so that the maximum voltage stress on either transistor can never be more than the maximum DC input voltage.

The further significant advantage is that there is no leakage inductance energy to be dissipated. Any energy stored in the leakage inductance is not lost by dissipation in some resistive element or in the power transistors. Instead, energy stored in the leakage inductance during the “on” time is fed back into  $V_{dc}$  via  $D1$  and  $D2$  when the transistors turn “off.” The leakage inductance current flows out of the no-dot end of  $N_p$ , through  $D2$ , into the positive end of  $V_{dc}$ , out of its negative end, and up through  $D1$  back into the dot end of  $N_p$ .

Examination of Figure 2.13 reveals that the core is always reset in a time equal to the “on” time. The reverse polarity voltage across  $N_p$  when the transistors are “off” is equal to the forward polarity voltage across it when the transistors are “on.” Thus the core will always be fully reset with a 20% safety margin before the start of a succeeding half cycle if the maximum “on” time is no greater than 80% of a half period. This is accomplished by choosing secondary turns so that the peak secondary voltage at minimum  $V_{dc}$  times the maximum duty cycle of 0.4 equals the desired output voltage (see Eq. 2.25).

### 2.4.1.1 Practical Output Power Limits

It should be noted that this topology still yields only one power pulse per period, just like the single-ended forward converter. Thus the power available from a specific core is pretty much the same for either the single- or double-ended configuration. As noted in Section 2.3.10.6, the reset winding in the single-ended circuit carries only magnetizing current during the power transistor “off” time. Since that current is

## Chapter 2: Push-Pull and Forward Converter Topologies 97

small, the reset winding can be wound with very small wire. Thus, the absence of a reset winding in the double-ended circuit does not permit significantly larger power winding wire size and output power from a given core.

Because the maximum off transistor voltage stress cannot be greater than the maximum DC input voltage, however, the 200-W practical power limit for the single-ended forward converter discussed in Section 2.3.7 does not hold for the double-ended forward converter. With the reduced voltage stress, output powers of 400 to 500 W are obtainable, and transistors with the required voltage and current capability and adequate gain are available at low price.

Consider a double-ended forward converter operating from a nominal 120-V AC line with  $\pm 10\%$  tolerance and  $\pm 15\%$  allowance for transients on top of that. The maximum rectified DC voltage is  $1.41 \times 120 \times 1.1 \times 1.15 = 214$  V, and the minimum rectified DC voltage is  $1.41 \times 120 \div 1.1 \div 1.15 = 134$  V, and equivalent flat-topped primary current from Eq. 2.28 is  $I_{pft} = 3.13 P_o / \underline{V}_{dc}$ , and for  $P_o = 400$  W,  $I_{pft} = 9.6$  A. This requirement can be satisfied quite easily, because both bipolar and MOSFET transistors with adequately high gain are available at low cost.

A double-ended forward converter with a voltage doubler from the 120-V AC line would be a better alternative (see Figure 3.1). This would double the voltage stress to 428 V but would halve the peak current to 4.8 A. With 4.8 A of primary current, RFI problems would be less severe. A bipolar transistor with a 400-V  $V_{ceo}$  rating could tolerate 428 V easily, with  $-1$ - to  $-5$ -V reverse bias at the instant of turn “off” ( $V_{cev}$  rating).

### 2.4.2 Design Relations and Transformer Design

#### 2.4.2.1 Core Selection—Primary Turns and Wire Size

The transformer design for the double-ended forward converter proceeds exactly as for the single-ended converter. A core is selected from the aforementioned selection charts (to be presented in Chapter 7 on magnetics) for the required output power and operating frequency.

The number of primary turns is chosen from Faraday’s law as in Eq. 2.40. There the minimum primary voltage is  $(\underline{V}_{dc} - 2)$  as there are two transistors rather than one in series with the primary—but the transistor drops are insignificant since  $\underline{V}_{dc}$  is usually 134 V (120 V AC). Maximum “on” time should be set at  $0.8T/2$  and  $dB$  at 1600 G up to 50 kHz, or higher if not limited by core losses.

As mentioned for frequencies from 100 to 300 kHz, peak flux density may have to be set from about 1400 to 800 G, as core losses increase with frequency. But the exact peak flux density chosen depends on



## 98 Switching Power Supply Design

whether the newer, lower-loss materials are available. It also depends to some extent on transformer size—smaller cores can generally operate at higher flux density, because they have a larger ratio of radiating surface area to volume and hence can get rid of the heat they generate (which is proportional to volume) more easily.

Since there is only one current or power pulse per period, as in the single-ended forward converter, the primary current for a given output power and minimum DC input voltage is given by Eq. 2.28, and the primary wire size is chosen from Eq. 2.42.

### 2.4.2.2 Secondary Turns and Wire Size

Secondary turns are chosen exactly as in Sections 2.3.2 and 2.3.3 from Eqs. 2.25 to 2.27. Wire sizes are calculated as in Section 2.3.10.5 from Eq. 2.44.

### 2.4.2.3 Output Filter Design

The output inductor and capacitor magnitudes are calculated exactly as in Section 2.3.11 from Eqs. 2.46 to 2.48.

---

## 2.5 Interleaved Forward Converter Topology

### 2.5.1 Basic Operation—Merits, Drawbacks, and Output Power Limits

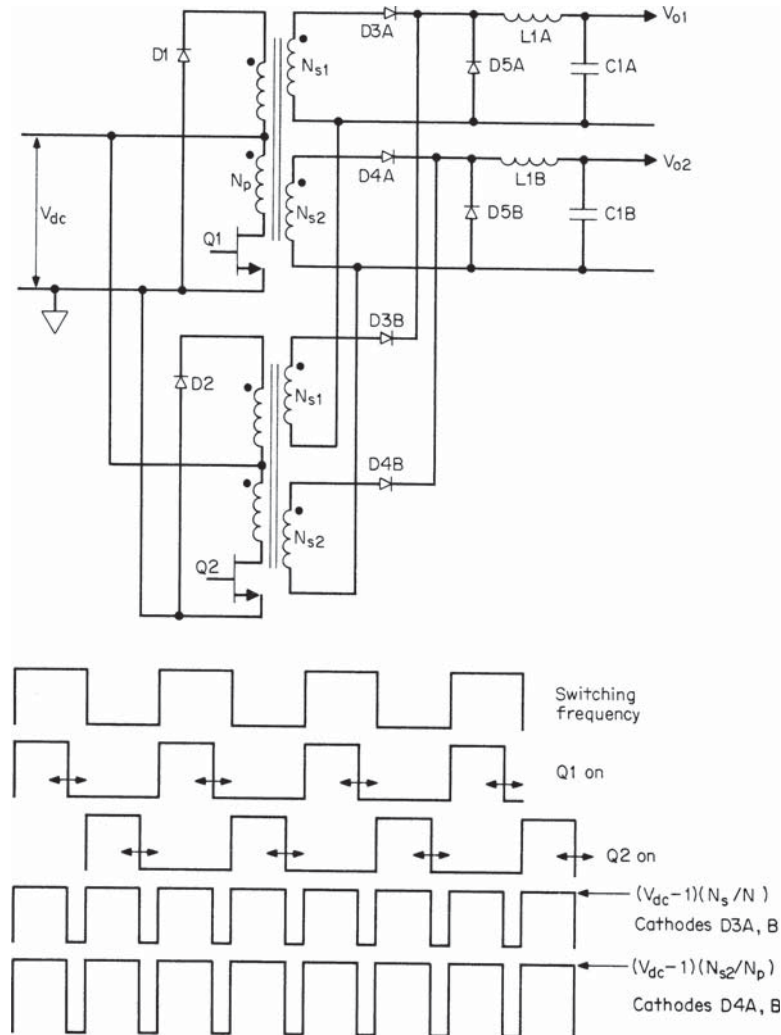
This topology is simply two identical single-ended forward converters operating on alternate half cycles with their secondary currents adding through rectifying “on” diodes. The topology is shown in Figure 2.14.

The advantage, of course, is that now there are two power pulses per period, as seen in Figure 2.14, reducing the ripple current; also each converter supplies only half the total output power.

Equivalent flat-topped peak transistor current is derived from Eq. 2.28 as  $I_{pft} = 3.13 P_{ot}/2V_{dc}$  where  $P_{ot}$  is the total output power. This transistor current is half that of a single forward converter at the same total output power. Thus the expense of two transistors is offset by the lower peak current rating and lower cost than that of the higher current rating device.

Looking at it another way, two transistors of the same current rating used at the same peak current as one single-ended converter at a given output power in an interleaved converter would yield twice the output power of the single converter.

Also, since the intensity of EMI generated is proportional to the peak current, not to the number of current pulses, an interleaved converter of the same total output power as a single forward converter will generate less EMI.



**FIGURE 2.14** Interleaved forward converter. Interleaving the “on” times of Q1 and Q2 on alternate half cycles, and summing their secondary outputs, gives two power pulses per period but avoids the flux-imbalance problem of the push-pull topology.

## 100 Switching Power Supply Design

If this topology is compared to a push-pull, it might be thought that the push-pull is preferable. Although both are two-transistor circuits, the two transformers in the interleaved forward converter are probably more expensive and occupy more space than a single large one in a push-pull circuit. But there is the ever-present uncertainty that the flux imbalance problem in the push-pull could appear under odd transient line and load conditions. The certainty that there is no flux imbalance in the interleaved forward converter is probably the best argument for its use.

There is one special, although not frequent, case where the interleaved forward converter is a much more desirable choice than a single forward converter of the same output power. This occurs when a DC output voltage is high—over about 200 V. In a single forward converter the peak reverse voltage experienced by the output free-wheeling diodes ( $D5A$  or  $D5B$ ) is twice that for an interleaved forward converter as the duty cycle in the latter is twice that in the former.

This is no problem when output voltages are low, as can be seen in Eq. 2.25. Transformer secondary turns are always selected (for the single forward converter) so that at minimum DC input, when the secondary voltage is at its minimum, the duty cycle  $T_{on}/T$  need not be more than 0.4 to yield the desired output voltage. Then for a DC output of 200 V, the peak reverse voltage experienced by the free-wheeling diode is 500 V. At the instant of power transistor turn “on,” the free-wheeling diode has been carrying a large forward current and will suddenly be subjected to reverse voltage. If the diode has slow reverse recovery time, it will draw a large reverse current for a short time at 500-V reverse voltage and run dangerously hot.

Diodes with larger reverse voltage ratings generally have slower recovery times and can be a serious problem. The interleaved forward converter runs at twice the duty cycle and, for a 200 V-DC output, subjects the free-wheeling diode to only 250 V. This permits a lower voltage, faster-recovery diode with considerably lower dissipation.

### 2.5.2 Transformer Design Relations

#### 2.5.2.1 Core Selection

The core for the two transformers will be selected from the aforementioned charts, to be presented in Chapter 7, but it will be chosen for half the total power output that each transformer must supply.

#### 2.5.2.2 Primary Turns and Wire Size

The number of primary turns in the interleaved forward converter is still given by Eq. 2.40, as each converter’s “on” time will still be  $0.8T/2$  at minimum DC input. The core iron area  $A_e$  will be read from

**Chapter 2: Push-Pull and Forward Converter Topologies 101**

the catalogs for the selected core. Primary wire size will be chosen from Eq. 2.42 at half the total output power.

**2.5.2.3 Secondary Turns and Wire Size**

The number of secondary turns will be chosen from Eqs. 2.26 and 2.27, but therein the duty cycle will be 0.8 as there are two voltage pulses, each of duration  $0.8T/2$  at  $V_{dc}$ . Wire size will still be chosen from Eq. 2.44, where  $I_{dc}$  is the actual DC output current that each secondary carries at a maximum duty cycle of 0.4.

**2.5.3 Output Filter Design****2.5.3.1 Output Inductor Design**

The output inductor sees two current pulses per period, exactly like the output inductor in the push-pull topology. These pulses have the same width, amplitude, and duty cycle as the push-pull inductor at the same DC output current. Hence the magnitude of the inductance is calculated from Eq. 2.20 as for the push-pull inductor.

**2.5.3.2 Output Capacitor Design**

Similarly, the output capacitor “doesn’t know” whether it is filtering a full-wave secondary waveform from a push-pull topology or from an interleaved forward converter. Thus for the same inductor current ramp amplitude and permissible output ripple as the push-pull circuit, the capacitor is selected from Eq. 2.22.

---

**Reference**

1. K. Billings, *Switchmode Power Supply Handbook*, New York: McGraw-Hill, 1990.

## Push-Pull and Forward Converter Topologies

# CHAPTER 3

---

## Half- and Full-Bridge Converter Topologies

---

### 3.1 Introduction

Half-bridge and full-bridge topologies stress their transistors to a voltage equal to the DC input voltage not to twice this value, as do the push-pull, single-ended, and interleaved forward converter topologies. Thus the bridge topologies are used mainly in offline converters where supply voltage would be more than the switching transistors could safely tolerate. Bridge topologies are almost always used where the normal AC input voltage is 220 V or higher, and frequently even for 120-V AC inputs.

An additional valuable feature of the bridge topologies is that primary leakage inductance spikes (Figures 2.1 and 2.10) are easily clamped to the DC supply bus and the energy stored in the leakage inductance is returned to the input instead of having to be dissipated in a resistive snubber element.

---

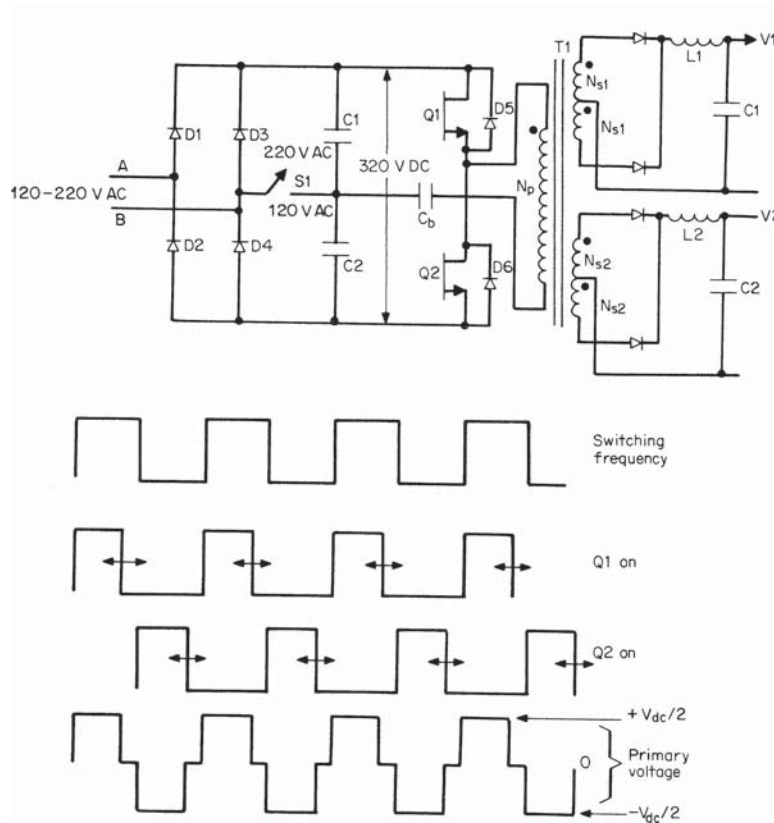
### 3.2 Half-Bridge Converter Topology

#### 3.2.1 Basic Operation

Half-bridge converter topology is shown in Figure 3.1. Its major advantage is that, like the double-ended forward converter, it subjects the “off” transistor to only  $V_{dc}$  and not twice that value. Thus it is widely used in equipment intended for the European market, where the AC input voltage is 220 V.

First consider the input rectifier and filter in Figure 3.1. It is used universally when the equipment is to work from either 120-V AC American power or 220-V AC European power. The circuit always yields roughly 320-V rectified DC voltage, whether the input is 120 or

## 104 Switching Power Supply Design



**FIGURE 3.1** Half-bridge converter. One end of the power transformer primary is connected to the junction of filter capacitors  $C_1$ ,  $C_2$  via a small DC locking capacitor  $C_b$ . The other end is connected to the junction of  $Q_1$ ,  $Q_2$ , which turn “on” and “off” on alternate half cycles. With  $S_1$  in the closed position, the circuit is a voltage doubler; in the open position, it is a full-wave rectifier. In either case, the rectified output is about 308 to 336  $V_{dc}$ .

220 V AC. It does this when switch  $S_1$  is set to the open position for 220-V AC input, or to the closed position for 120-V AC input. The  $S_1$  component is normally not a switch; more often it is a wire link that is either installed for 120 V AC, or not for 220 V AC.

With the switch in the open 220-V AC position the circuit is a full-wave rectifier, with filter capacitors  $C_1$  and  $C_2$  in series. It produces a peak rectified DC voltage of about  $(1.41 \times 220) - 2$  or 308 V. When the switch is in the closed 120-V AC position, the circuit acts as a voltage doubler. On a half cycle of the input voltage when  $A$  is positive relative

to  $B$ ,  $C1$  is charged positively via  $D1$  to a peak of  $(1.41 \times 120) - 1$  or 168 V. On a half cycle when  $A$  is negative with respect to  $B$ , capacitor  $C2$  is charged positively via  $D2$  to 168 V. The total voltage across  $C1$  and  $C2$  in series is then 336 V. It can be seen in Figure 3.1 that with either transistor “on,” the “off” transistor is subjected to the maximum DC input voltage and not twice that value.

Since the topology subjects the “off” transistor to only  $V_{dc}$  and not  $2V_{dc}$ , there are many inexpensive bipolar and MOSFET transistors that can support the nominal 336 DC V plus 15% upper maximum of 386 V. Thus the equipment can be used with either 120- or 220-V AC line inputs by making a simple switch or linkage change.

**After Pressman** *An automatic line voltage sensing and switching circuit that drives a relay or other device in the position of  $S1$  is sometimes implemented. The added cost and circuit complexity is offset by making the switching action transparent to the end user of the equipment and by preventing the possible damaging error of running the supply at 220 V while connected for 120 V. ~ T.M.*

Assuming a nominal rectified DC voltage of 336 V, the topology works as follows: For the moment, ignore the small series blocking capacitor  $C_b$ . Assume the bottom end of  $N_p$  is connected to the junction of  $C1$  and  $C2$ . Then if the leakages in  $C1$ ,  $C2$  are assumed to be equal, that point will be at half the rectified DC voltage, about 168 V. It is generally good practice to place equal bleeder resistors across  $C1$  and  $C2$  to equalize their voltage drops. Now  $Q1$  and  $Q2$  conduct on alternate half cycles. When  $Q1$  is “on” and  $Q2$  “off” (Figure 3.1), the dot end of  $N_p$  is 168 V positive with respect to its no-dot end, and the “off” stress on  $Q2$  is only 336 V. When  $Q2$  is “on” and  $Q1$  “off,” the dot end of  $N_p$  is 168 V negative with respect to its no-dot end and the emitter of  $Q1$  is 336 V negative with respect to its collector.

This AC square-wave primary voltage produces full-wave square waveshapes on all secondaries—exactly like the secondary voltages in the push-pull topology. The selection of secondary voltages and wire sizes and the output inductor and capacitor proceed exactly as for the push-pull circuit.

### 3.2.2 Half-Bridge Magnetics

#### 3.2.2.1 Selecting Maximum “On” Time, Magnetic Core, and Primary Turns

It can be seen in Figure 3.1, that if  $Q1$  and  $Q2$  are “on” simultaneously—even for a very short time—there is a short circuit across the supply voltage and the transistors will be destroyed. To make sure that this does not happen, the maximum  $Q1$  or  $Q2$  “on”



## 106 Switching Power Supply Design

time, which occurs at minimum DC supply voltage, will be set at 80% of a half period. The secondary turns will be chosen so that the desired output voltages are obtained with an “on” time of no more than  $0.8T/2$ . An “on”-time clamp will be provided to ensure that the “on” time can never be greater than  $0.8T/2$  under fault or transient conditions.

The core is selected from the tables in Chapter 7 mentioned earlier. These tables give maximum available output power as a function of operating frequency, peak flux density, core and iron areas, and coil current density.

With a core selected and its iron area known, the number of primary turns is calculated from Faraday’s law (Eq. 1.17) using the minimum primary voltage  $(V_{dc}/2) - 1$ , and the maximum “on” time of  $0.8T/2$ . Here, the flux excursion  $dB$  in the equation is twice the desired peak flux density (1600 G below 50 kHz, or less at higher frequency), because the half-bridge core operates in the first and third quadrants of its hysteresis loop—unlike the forward converter (Section 2.3.9), which operates in the first quadrant only.

### 3.2.2.2 The Relation Between Input Voltage, Primary Current, and Output Power

If we assume an efficiency of 80%, then

$$P_{in} = 1.25P_o$$

The input power at minimum supply voltage is the product of minimum primary voltage and average primary current at minimum DC input. At minimum DC input, the maximum “on” time in each half period will be set at  $0.8T/2$  as discussed above, and the primary has two current pulses of width  $0.8T/2$  per period  $T$ . At primary voltage  $V_{dc}/2$ , the input power is  $1.25P_o = (V_{dc}/2)(I_{pft})(0.8T/T)$ , where  $I_{pft}$  is the peak equivalent flat-topped primary current pulse. Then

$$I_{pft} \text{ (half bridge)} = \frac{3.13P_o}{V_{dc}} \quad (3.1)$$

### 3.2.2.3 Primary Wire Size Selection

Primary wire size must be much larger in a half bridge than in a push-pull circuit of the same output power. However, there are two half primaries in the push-pull, each of which has to support twice the voltage of the half-bridge primary when operated from the same supply voltage. Consequently, coil sizes for the two topologies are not much different. Half-bridge primary RMS current is

$$I_{rms} = I_{pft} \sqrt{0.8T/T}$$

## Chapter 3: Half- and Full-Bridge Converter Topologies 107

and from Eq. 3.1

$$I_{\text{rms}} = \frac{2.79 P_o}{V_{\text{dc}}} \quad (3.2)$$

At 500 circular mils per RMS ampere, the required number of circular mils is

$$\begin{aligned} \text{Circular mils needed} &= \frac{500 \times 2.79 P_o}{V_{\text{dc}}} \\ &= \frac{1395 P_o}{V_{\text{dc}}} \end{aligned} \quad (3.3)$$

### 3.2.2.4 Secondary Turns and Wire Size Selection

In the following treatment the number of secondary turns will be selected using Eqs. 2.1 to 2.3 for  $\overline{T_{\text{on}}} = 0.8T/2$ , and the term  $V_{\text{dc}} - 1$  will be replaced by the minimum primary voltage, which is  $(V_{\text{dc}}/2) - 1$ . The secondary RMS currents and wire sizes are calculated from Eqs. 2.13 and 2.14, exactly as for the full-wave secondaries of a push-pull circuit.

### 3.2.3 Output Filter Calculations

The output inductor and capacitor are selected using Eqs. 2.20 and 2.22 as in a push-pull circuit for the same inductor current ramp amplitude and desired output ripple voltage.

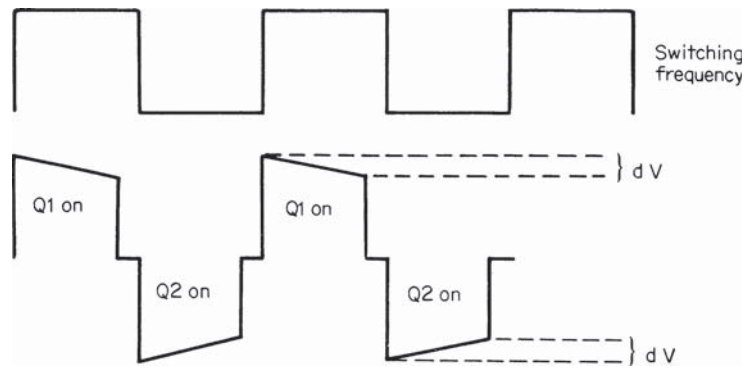
### 3.2.4 Blocking Capacitor to Avoid Flux Imbalance

To avoid the flux-imbalance problem discussed in connection with the push-pull circuit (Section 2.2.5), a small capacitor  $C_b$  is fitted in series with the primary as in Figure 3.1. Recall that flux imbalance occurs if the volt-second product across the primary while the core is set (moves in one direction along the hysteresis loop) differs from the volt-second product after it moves in the opposite direction.

Thus, if the junction of C1 and C2 is not at exactly half the supply voltage, the voltage across the primary when Q1 is "on" will differ from the voltage across it when Q2 is "on" and the core will walk up or down the hysteresis loop, eventually causing saturation and destroying the transistors.

This saturating effect comes about because there is an effective DC current bias in the primary. To avoid this DC bias, the blocking capacitor is placed in series in the primary. The capacitor value is selected

## 108 Switching Power Supply Design



**FIGURE 3.2** The small blocking capacitor  $C_b$  in series with the half-bridge primary (Figure 3.1) is needed to prevent flux imbalance if the junction of the filter capacitors is not at exactly the midpoint of the supply voltage. Primary current charges the capacitor, causing a droop in the primary voltage waveform. This droop should be kept to no more than 10%. (The droop in primary voltage, due to the offset charging of the blocking capacitor, is shown as  $dV$ .)

as follows. The capacitor charges up as the primary current  $I_{pft}$  flows into it, robbing voltage from the flat-topped primary pulse shown in Figure 3.2.

This DC offset robs volt-seconds from all secondary windings and forces a longer “on” time to achieve the desired output voltage. In general, it is desirable to keep the primary voltage pulses as flat-topped as possible.

In this example, we will assume a permissible droop of  $dV$ . The equivalent flat-topped current pulse that causes this droop is  $I_{pft}$  in Eq. 3.1. Then, because that current flows for  $0.8T/2$ , the required capacitor magnitude is simply

$$C_b = \frac{I_{pft} \times 0.8T/2}{dV} \quad (3.4)$$

Consider an example assuming a 150-W half bridge operating at 100 kHz from a nominal DC input of 320 V. At 15% low line, the DC input is 272 V and the primary voltage is  $\pm 272/2$  or  $\pm 136$  V.

A tolerable droop in the flat-topped primary voltage pulse would be 10% or about 14 V.

Then from Eq. 3.1 for 150 W and  $V_{dc}$  of 272 V,  $I_{pft} = 3.13 \times 150/272 = 1.73$  A, and from Eq. 3.4,  $C_b = 1.73 \times 0.8 \times 5 \times 10^{-6}/14 = 0.49 \mu\text{F}$ . The capacitor must be a nonpolarized type.

### 3.2.5 Half-Bridge Leakage Inductance Problems

Leakage inductance spikes, which are so troublesome in the single-ended forward converter and push-pull topology, are easily avoided in the half bridge: they are clamped to  $V_{dc}$  by the clamping diodes  $D5$ ,  $D6$  across transistors  $Q1$ ,  $Q2$ .

Assuming  $Q1$  is “on,” the load and magnetizing currents flow through it and through the primary leakage inductance of  $T1$ , the paralleled  $T1$  magnetizing inductance, and the secondary load impedances that are reflected by their turn ratios squared into the primary. Then it flows through  $C_b$  into the  $C1$ ,  $C2$  junction. The dot end of  $N_p$  is positive with respect to its no-dot end.

When  $Q1$  turns “off,” the magnetizing inductance forces all winding polarities to reverse. The dot end of  $T1$  starts to go negative by flyback action, and if this were to continue, it would put more than  $V_{dc}$  across  $Q1$  and could damage it. Also,  $Q2$  could be damaged by imposing a reverse voltage across it. However, the dot end of  $T1$  is clamped by diode  $D6$  to the supply rail  $V_{dc}$  and can go no more negative than the negative end of the supply.

Similarly, when  $Q2$  is “on,” it stores current in the magnetizing inductance, and the dot end of  $N_p$  is negative with respect to the no-dot end (which is close to  $V_{dc}/2$ ). When  $Q2$  turns “off,” the magnetizing inductance reverses all winding polarities by flyback action and the dot end of  $N_p$  tries to go positive but is caught at  $V_{dc}$  by clamp diode  $D5$ . Thus the energy stored in the leakage inductance during the “on” time is returned to the supply rail  $V_{dc}$  via diodes  $D5$ ,  $D6$ .

### 3.2.6 Double-Ended Forward Converter vs. Half Bridge

Both the half-bridge and double-ended forward converter (Figure 2.13) subject their respective “off” state transistors to only  $V_{dc}$  and not twice that. Thus, they are both candidates for the European market where the prime power is 220 V AC. Both methods have been used in such applications in enormous numbers, and it is instructive to consider the relative merits and drawbacks of each approach.

The most significant difference between the two approaches is that the half-bridge secondary provides full-wave output as compared with half-wave in the forward converter. Thus, the square-wave frequency in the half-bridge secondary is twice that in the forward converter, and hence, the output  $LC$  inductor and capacitor are smaller with the half bridge.

**After Pressman** *The term frequency, when applied to double-ended and single-ended converters, is not helpful. It is easier to consider secondary pulse*

## 110 Switching Power Supply Design

repetition rate. If the pulse rate is the same for both types (conventionally, doubling the frequency of the single-ended case), the power throughput will be the same. It is just a matter of convention rather than a basic difference in power ratings. In the push-pull case, each positive and negative half cycle produces an output pulse resulting in two pulses per cycle (pulse frequency doubling). So simply producing two pulses from the single-ended topology in the same time period results in the same output.

The real difference between the two is that the push-pull takes the flux in the core from a negative position on the BH loop to a positive position and, conversely, while the single-ended goes from zero to positive only. Potentially the push-pull has twice the flux range. However, above about 50 kHz, the p-p flux swing is limited by core loss to less than 200 mT typically, a flux swing that can be obtained easily from both the push-pull and single-ended topologies. ~K.B.

Peak secondary voltages are higher with the forward converter because the duty cycle is half that of the half bridge. This is significant only if DC output voltages are high—greater than 200 V, as discussed in Section 2.5.1.

There are twice as many turns on the forward converter primary as on the half bridge because the former must sustain the full supply voltage as compared with half that voltage in the half bridge. Having fewer turns on the half-bridge primary may reduce its winding cost and result in lower parasitic capacities.

**After Pressman** *Although there are less turns on the half bridge, the current is doubled and copper loss is proportional to  $I^2$ , so the wire must be twice the diameter for the same copper loss. ~K.B.*

One final marginal factor in favor of the half bridge is that the coil losses in the primary due to the proximity effect (Section 7.5.6.1) are slightly lower than in the forward converter.

Proximity effect losses are caused by eddy currents induced in one winding layer by currents in adjacent layers. Proximity losses increase rapidly with the number of winding layers, and the forward converter may have more layers. The half-bridge primary has half the turns of a double-ended forward converter primary of equal output power operating from the same DC supply voltage. However, this is balanced somewhat by the larger wire size required for the half bridge. Thus, the required number of circular mils for a forward converter primary is given by Eq. 2.42 as  $985P_o/V_{dc}$  and for a half bridge by Eq. 3.3 as  $1395P_o/V_{dc}$ .

In a practical case, the lower proximity effect losses for the half bridge may be only a marginal advantage. Proximity effect losses will be discussed in more detail in Chapter 7.

### 3.2.7 Practical Output Power Limits in Half Bridge

Peak primary current and maximum transistor off-voltage stress determine the practical maximum available output power in the half bridge. This limit is about 400 to 500 W for a half bridge operating from 120-V AC input in the voltage-doubling mode, shown in Figure 3.1. It is equal to that required for the double-ended forward converter as discussed in Section 2.4.1.1 and which can be seen as follows: The peak equivalent flat-topped primary current is given by Eq. 3.1 as  $I_{\text{pft}} = 3.13P_o/V_{\text{dc}}$ . For a  $\pm 10\%$  steady-state tolerance and a 15% transient allowance on top of that, the maximum off-voltage stress is  $V_{\text{dc}} = 1.41 \times 120 \times 2 \times 1.1 \times 1.15$  or 428 V. The minimum DC input voltage is  $V_{\text{dc}} = 1.41 \times 120 \times 2/1.1/1.15 = 268$  V.

Thus, for 500-W output, Eq. 3.1 gives the peak primary current as  $I_{\text{pft}} = 3.13 \times 500/268 = 5.84$  A, and there are many transistor choices—either MOSFETs or bipolars—with 428-V, 6-A ratings. Bipolars must have a  $-1$ -V to  $-5$ -V reverse bias (to permit  $V_{\text{cev}}$  rating) at turn “off” to permit a safe “off” voltage of 428 V. Most adequately fast transistors at that current rating have a  $V_{\text{ceo}}$  rating of only 400 V.

The half bridge can be pushed to 1000-W output, but at the required 12-A rating, most available bipolar transistors with adequate speed have too low a gain. MOSFET transistors at the required current and voltage rating have too large an “on” drop and are too expensive for most commercial applications at the time of this writing.

Above 500 W, consider the full-bridge topology, a small modification of the half bridge but capable of twice the output power.

## 3.3 Full-Bridge Converter Topology

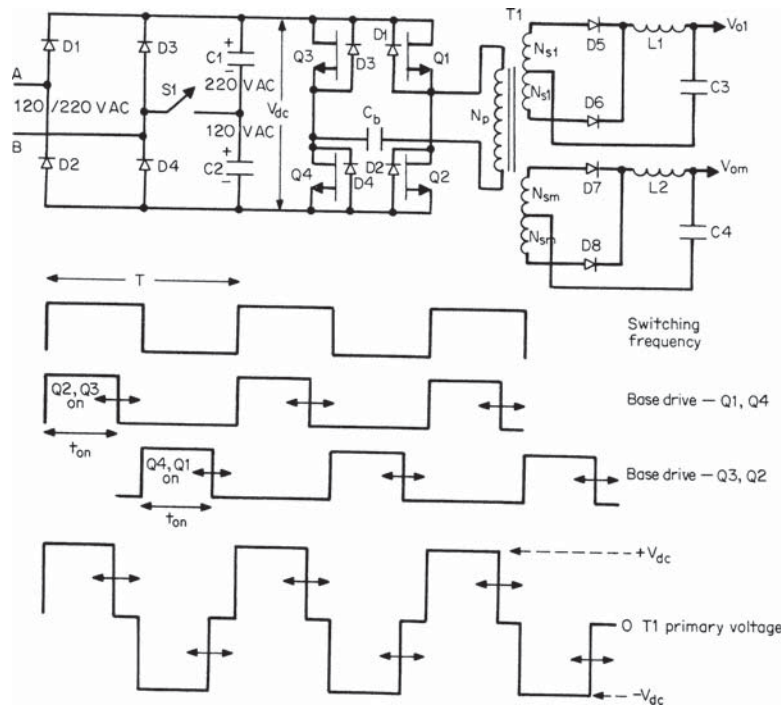
### 3.3.1 Basic Operation

The full-bridge converter topology is shown in Figure 3.3 with the same voltage-doubling full-wave bridge rectifying scheme as was shown for the half bridge (Section 3.2.1). It can be used as an offline converter from a 440-V AC line.

Its major advantage is that the voltage impressed across the primary is a square wave of  $\pm V_{\text{dc}}$ , instead of  $\pm V_{\text{dc}}/2$  for the half bridge. Further, the maximum transistor off-voltage stress is only the maximum DC input voltage—just as for the half bridge. Thus, for transistors of the same peak current and voltage ratings, the full bridge is able to deliver twice the output power of the half bridge.

In the full bridge the transformer primary turns must be twice that of the half bridge as the primary winding must sustain twice the voltage. However, to get the same output power as a half bridge from the

## 112 Switching Power Supply Design



**FIGURE 3.3** Full-bridge converter topology. Power transformer  $T1$  is bridged between the junction of  $Q1$ ,  $Q2$  and  $Q3$ ,  $Q4$ . Transistors  $Q2$ ,  $Q3$  are switched “on” simultaneously for an adjustable time during one half period; then transistors  $Q4$ ,  $Q1$  are simultaneously “on” for an equal time during the alternate half period. Transformer primary voltage is a square wave of  $\pm V_{dc}$ . This contrasts with the  $\pm V_{dc}/2$  primary voltage in the half bridge and yields twice the available power.

same DC supply voltage, the peak and RMS currents are half that of the half bridge because the transformer primary supports twice the voltage as the half bridge. With twice the primary turns but half the RMS current, the full-bridge transformer size is identical to that of the half bridge at equal output powers. With a larger transformer, the full bridge can deliver twice the output of the half bridge with transistors of identical voltage and current ratings.

Figure 3.3 shows a master output,  $V_{om}$  and a single slave output,  $V_{o1}$ . The circuit works as follows. Diagonally opposite transistors ( $Q2$  and  $Q3$  or  $Q4$  and  $Q1$ ) are turned “on” simultaneously during alternate half cycles. Assuming that the “on” drop of the transistors is negligible, the transformer primary is thus driven with an alternating polarity



square wave of amplitude  $V_{dc}$  and “on” time  $t_{on}$  determined by the feedback loop.

The feedback loop senses a fraction of  $V_{om}$ , and the pulse width modulator controls  $t_{on}$  so as to keep  $V_{om}$  constant against line and load changes. The slave outputs, as in all other topologies, are kept constant against AC line input changes, but only to within about 5 to 8% against load changes. If we assume a 1-V “on” drop in each switching transistor, 0.5-V forward drop in the master output Schottky rectifiers, and 1.0-V forward drops in the slave output rectifiers, we get

$$V_{om} = \left[ (V_{dc} - 2) \frac{N_{sm}}{N_p} - 0.5 \right] \frac{2t_{on}}{T} \quad (3.5a)$$

$$V_{om} \approx V_{dc} \frac{N_{sm}}{N_p} \frac{2t_{on}}{T} \quad (3.5b)$$

$$V_{o1} = \left[ (V_{dc} - 2) \frac{N_{s1}}{N_p} - 1 \right] \frac{2t_{on}}{T} \quad (3.6a)$$

$$V_{o1} \approx V_{dc} \frac{N_{s1}}{N_p} \frac{2t_{on}}{T} \quad (3.6b)$$

As in all pulse width modulated regulators, as  $V_{dc}$  goes up or down by a given percentage, the width modulator decreases or increases the “on” time by the same percentage so as to keep the product  $(V_{dc})(t_{on})$  and, hence, the output voltages constant.

### 3.3.2 Full-Bridge Magnetics

#### 3.3.2.1 Maximum “On” Time, Core, and Primary Turns Selection

In Figure 3.3, it can be seen that if two transistors that are vertically stacked above one another ( $Q3$  and  $Q4$ , or  $Q1$  and  $Q2$ ) are turned “on” simultaneously, they would present a dead short-circuit across the DC supply bus and the transistors would fail. To ensure this does not happen, the maximum “on” time  $\overline{t_{on}}$  will be chosen as 80% of a half period. This is “chosen” by selecting the turns ratios  $N_{sm}/N_p$ ,  $N_{s1}/N_p$ , so that in those equations for  $\underline{V_{dc}}$ , with  $\overline{t_{on}}$  equal to  $0.8T/2$ , the correct output voltages— $V_{om}$ ,  $V_{o1}$ —are obtained. The maximum “on” time occurs at minimum DC input voltage  $\underline{V_{dc}}$ —as can be seen in Eqs. 3.5b and 3.6b.

The magnetic core and operating frequency are chosen from the core-frequency selection chart in Chapter 7. With a core selected and its iron area  $A_e$  known, the number of primary turns  $N_p$  is chosen from Faraday’s law (Eq. 1.17). In Eq. 1.17,  $E$  is the minimum primary voltage  $(\underline{V_{dc}} - 2)$ , and  $dB$  is the flux change desired in the time  $dt$  of  $0.8T/2$ . As discussed in Section 2.2.9.4,  $dB$  will be chosen as 3200 G



## 114 Switching Power Supply Design

(−1600 to +1600 G) for frequencies up to 50 kHz and this will be reduced at higher frequencies because core losses increase.

### 3.3.2.2 Relation Between Input Voltage, Primary Current, and Output Power

Assume an efficiency of 80% from the primary input to the total output power. Then

$$P_o = 0.8P_{in} \quad \text{or} \quad P_{in} = 1.25P_o$$

At minimum DC input voltage  $\underline{V_{dc}}$ , on time per half period is  $0.8T/2$ , and duty cycle over a complete period is 0.8. Then neglecting the power transistor on drops, input power at  $\underline{V_{dc}}$  is

$$P_{in} = \underline{V_{dc}}(0.8)I_{pft} = 1.25P_o$$

or

$$I_{pft} = \frac{1.56P_o}{\underline{V_{dc}}} \quad (3.7)$$

where  $I_{pft}$  is the equivalent primary flat-topped current as described in Section 2.2.10.1.

### 3.3.2.3 Primary Wire Size Selection

Current  $I_{pft}$  flows at a duty cycle of 0.8 so its RMS value is

$$I_{rms} = I_{pft}\sqrt{0.8}.$$

Then, from Eq. 3.7

$$\begin{aligned} I_{rms} &= (1.56P_o/\underline{V_{dc}})\sqrt{0.8} \\ I_{rms} &= \frac{1.40P_o}{\underline{V_{dc}}} \end{aligned} \quad (3.8)$$

And at a current density of 500 circular mils per RMS ampere, the required number of circular mils is

$$\begin{aligned} \text{Circular mils needed} &= \frac{500 \times 1.40P_o}{\underline{V_{dc}}} \\ &= \frac{700P_o}{\underline{V_{dc}}} \end{aligned} \quad (3.9)$$

### 3.3.2.4 Secondary Turns and Wire Size

The number of turns on each secondary is calculated from Eqs. 3.5a and 3.5b, where  $\overline{f_{on}}$  is  $0.8T/2$  for the specified minimum DC input

$V_{dc}$ ,  $N_p$  as calculated in Section 3.3.2.1, and all DC outputs are specified.

Secondary RMS currents and wire sizes are chosen exactly as for the push-pull secondaries as described in Section 2.2.10.3. The secondary RMS currents are given by Eq. 2.13 and the required circular mils for each half secondary is given by Eq. 2.14.

### 3.3.3 Output Filter Calculations

For the half-bridge and push-pull topologies that have full-wave output rectifiers, the output inductor and capacitors are calculated from Eqs. 2.20 and 2.22. Equation 2.20 specifies the output inductor for minimum DC output currents equal to one-tenth the nominal values. Equation 2.22 specifies the output capacitor for the specified peak-to-peak output ripple  $V_r$  and the selected peak-to-peak inductor current ripple amplitude.

### 3.3.4 Transformer Primary Blocking Capacitor

Figure 3.3 shows a small nonpolarized blocking capacitor  $C_b$  in series with the transformer. It is needed to avoid the flux-imbalance problem as discussed in Section 3.2.4.

Flux imbalance in the full bridge is less likely than in the half bridge, but still is possible. With bipolars, an “on” pair in one half cycle may have different storage times than the pair in the alternate half cycle. With MOSFETs, the “on” state voltage drops of the pairs for alternate half cycles may be unequal. In either case, if the volt-second product applied to the transformer primary in alternate half cycles is unequal, the core could walk off the center of the hysteresis loop, saturate the core, and destroy the transistors.

## Half- and Full-Bridge Converter Topologies

# CHAPTER 4

---

## Flyback Converter Topologies

---

### Foreword

I find that many engineers and students have great difficulty with the design of flyback type converters. This is unfortunate because these topologies are very useful, and, in fact, they are not difficult to design.

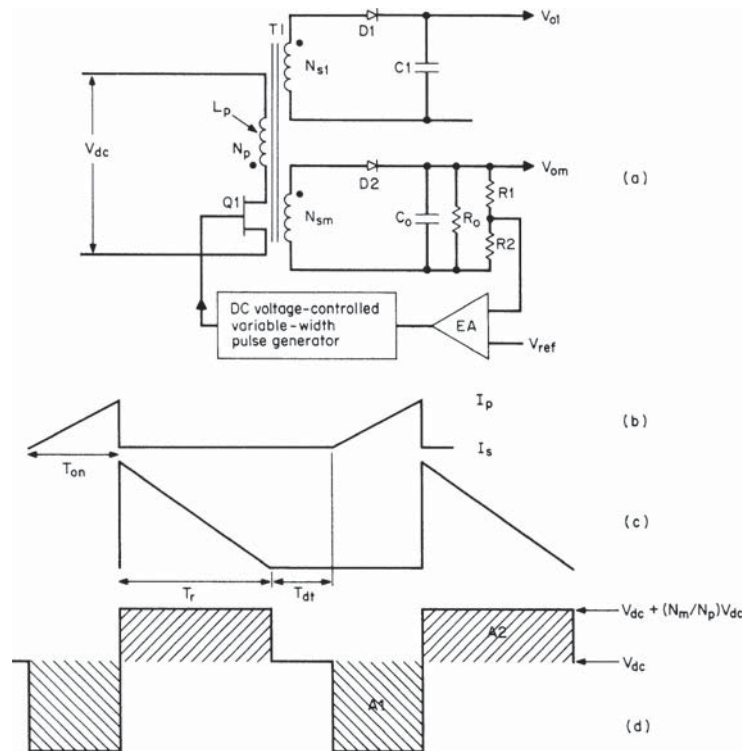
The problem is not the intrinsic difficulty of the subject matter (or the ability of the student). The fault is related to the way the subject is traditionally taught.

Right from the start the normal term *flyback transformer* immediately projects the wrong mindset. Not unreasonably, designers set out to design a “flyback transformer” as if it were a real transformer. This is not the way to go.

We are all very familiar with transformers, very simple devices really—we put a voltage across a primary winding and we get a voltage on a secondary winding. The voltage ratio follows the turns ratio, irrespective of the output (or load) current. In other words, the transformer conserves the voltage transfer ratio (one volt per turn on the primary results in one volt per turn on the secondary. You want ten volts? Then use ten turns, very simple). However, notice an important property of transformers, the primary and secondary conduct at the same time. If current flows into the start of the primary winding it flows out of the start of the secondary winding at the same time.

Figure 4.1 shows the basic schematic of a flyback converter. Notice the when Q1 is “on” current flows into the primary winding of *T1* but the secondary diodes are not conducting and there is no secondary current. When Q1 turns “off” the primary current stops, all winding voltages reverse by flyback action, and the output diodes and secondary windings now conduct current. So the primary and secondary windings in the flyback “transformer” conduct current at different times. This apparently minor difference dramatically changes the rules.

## 118 Switching Power Supply Design



**FIGURE 4.1** Basic flyback converter schematic. The action is as follows: When Q1 turns “on,” all rectifier diodes become reverse-biased, and all output load currents are supplied from the output capacitors. T1 acts like a pure inductor and primary current builds up linearly in it to a peak  $I_p$ . When Q1 turns “off,” all winding voltages reverse under flyback action, bringing the output diodes into conduction and the primary stored energy  $1/2LI_p^2$  is delivered to the output to supply load current and replenish the charge on the output capacitors (the charge that they lost when Q1 was on). The circuit is discontinuous if the secondary current has decayed to zero before the start of the next turn “on” period of Q1.

Think about it! When Q1 is “on” only the primary winding is conducting (the other windings are not visible to the primary because they are not conducting). Q1 thinks it is driving an inductor. When Q1 turns “off” only the secondary windings conduct and now the primary winding cannot be seen by the secondaries (so now the secondaries think they are being driven by an inductor). So how does this change the rules? Well, functionally the so-called flyback “transformer” is really functioning as an inductor with several windings and follows the rules applicable to inductors.

The rules for an inductor with more than one winding are as follows: The primary to secondary ampere-turns ratios are conserved (not the voltage ratios, as was the case with a true transformer). For example, if the primary is, say, 100 turns and the current when Q1 turns “off” is 1 amp, then we have developed 100 ampere-turns in the primary. This must be conserved in the secondaries. With, say, a single secondary winding of 10 turns, the secondary current will be 10 amps ( $10T \times 10A = 100$  ampere-turns). In the same way, a single turn will develop 100 amps or 1000 secondary turns will develop 0.1 amps.

So where do we stand with regard to voltage? Well, to the first order, there is no correlation between primary and secondary voltages. The secondary voltage is simply a function of load. Consider the 10-turn 10-amp (100 ampere-turns) secondary winding example mentioned above. If we terminate the winding with a 1-ohm load, we will get 10 volts. What is more striking because the 10 amps must be conserved is that if we terminate it with 100 ohms, we will get 1000 volts! This is why the flyback topology is so useful for generating high voltages (don’t try to open circuit this winding because it will destroy the semiconductors). With several secondary windings conducting at the same time, then the sum of all the secondary ampere-turns must be conserved.

So the lesson we learn here is that flyback “transformers” actually operate as inductors and must be designed as such. (In Chapter 7, I use the term *choke* instead of inductor because the core must support both DC and AC components of current.) If flyback “transformers” had originally been called by their correct functional name, “flyback chokes,” then a lot of confusion could have been avoided.

We must not forget that voltage transformation is still taking place between primary and secondary windings even if they are not conducting at the same time. Taking the above example of 10 turns terminated in 100 ohms, the 1000 volts thus developed on this secondary winding will reflect back to the primary as 10,000 volts; this added to the supply of 100 volts will stress Q1 in its “off” state with 10,100 volts (where did I put that 11,000 volt transistor?). Hardly practical, but the theory holds.

So when designing flyback transformers keep the following key points in mind:

1. Remember you are not designing a transformer, you are designing a choke with additional windings.
2. The primary turns are selected to satisfy the AC voltage stress (volt-seconds) and the core AC saturation properties:

$$N_p = \frac{VT}{BA_e}$$

## 120 Switching Power Supply Design

Where  $N_p$  is minimum primary turns

$V$  is the maximum primary DC voltage (volts)

$T$  is the maximum "on" period for Q1 (microseconds)

$B$  is the AC p-p flux swing (tesla) typically 200 mT for ferrite

$A_e$  is the effective center pole area of the core (mm<sup>2</sup>)

3. The secondary turns are optional. If you choose the same volts per turn on the secondary as was used for the primary, then the flyback voltage on Q1 will be twice the supply voltage.
4. When using a gapped ferrite core, the minimum core gap must be such that the core will not saturate for the sum of DC and AC magnetization current. More often the gap is chosen to satisfy the power transfer requirements. This normally results in a gap exceeding the minimum requirements. Remember the energy stored in the primary is

$$E(\text{joules}) = \frac{1}{2}LI^2$$

Remember this is the maximum energy that can be transferred to the secondary, and then only in the discontinuous (complete energy transfer) mode. In the continuous mode, only part of this energy is transferred.

**Note** *Although reducing the inductance  $L$  may appear to reduce the stored energy, the current  $I$  increases in the same ratio as the inductance decreases. Since the  $I$  parameter is squared, the stored energy actually increases as  $L$  decreases.*

5. It is not recommended that you try to design for a defined inductance. It is better to let inductance be a dependant variable as changing the core gap or core material (permeability) will change the inductance.

Below in Chapter 4, Pressman follows the conventional "flyback transformer" approach, providing a very complete analysis. The reader may find it helpful to first read Chapter 7 in this book and Part 2, Chapters 1 and 2 in my book, shown as Reference 1 at the end of this chapter.

---

### 4.1 Introduction

All the topologies previously discussed (with the exception of the boost regulator Section 1.4 and the polarity inverter Section 1.5) deliver power to their loads during the period when the power transistor is turned "on."

However, the flyback topologies described in this chapter operate in a fundamentally different way. During the power transistor “on” time, they store energy in the power transformer. During this period, the load current is supplied from an output filter capacity only. When the power transistor turns “off,” the energy stored in the power transformer is transferred to the load and to the output filter capacitor as it replaces the charge it lost when it alone was delivering load current.

The flyback has advantages and limitations, discussed in more detail later. A major advantage is that the output filter inductors normally required for all forward topologies are not required for flyback topologies because the transformer serves both functions. This is particularly valuable in low-cost multiple output power supplies yielding a significant saving in cost and space.

---

## 4.2 Basic Flyback Converter Schematic

The basic flyback converter topology together with typical current and voltage waveforms is shown in Figure 4.1. It is very widely used for low-cost applications in the power range from about 150 W down to less than 5 W. Its great initial attraction is immediately clear—it has no secondary output inductor, and the consequent saving in cost and volume is a significant advantage.

In Figure 4.1, flyback operation can be easily recognized from the position of the dots on the transformer primary and secondary (these dots show the starts of the windings). When  $Q1$  is “on,” the dot ends of all windings are negative with respect to their no-dot ends. Output rectifier diodes  $D1$  and  $D2$  are reverse-biased and all the output load currents are supplied from storage filter capacitors  $C1$  and  $C2$ . These will be chosen as described below to deliver the load currents with the maximum specified ripple or droop in output voltages.

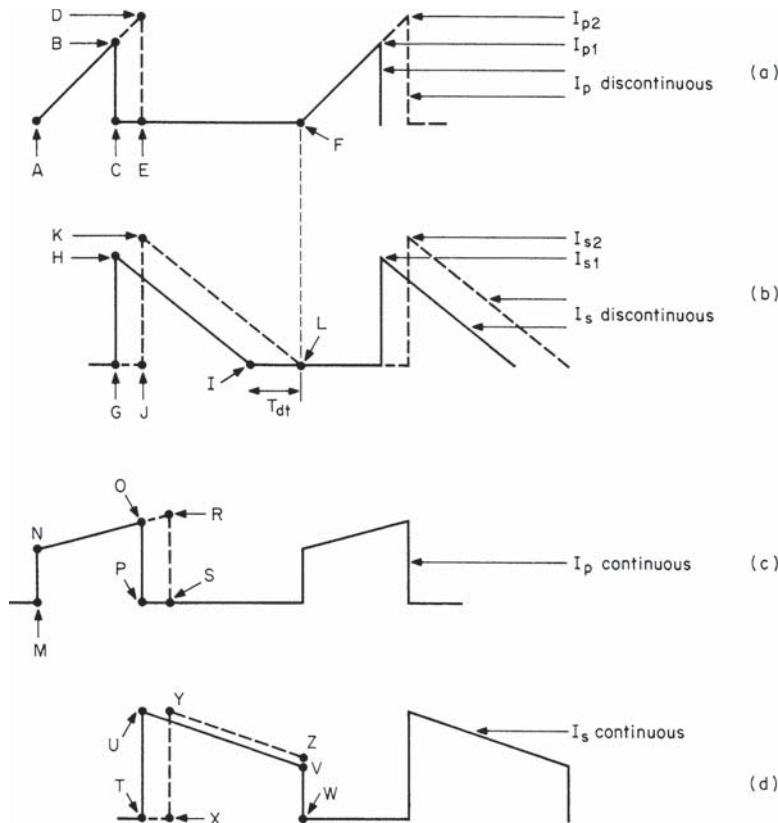
---

## 4.3 Operating Modes

There are two distinctly different operating modes for flyback converters: the continuous mode and the discontinuous mode. The waveforms, performance, and transfer functions are quite different for the two modes, and typical waveforms are shown in Figure 4.2. The value of primary inductance and the load current determine the mode of operation.



## 122 Switching Power Supply Design



**FIGURE 4.2** (a and b) Waveforms of a discontinuous-mode flyback at the point of transition to continuous-mode operation. Notice in the discontinuous mode, the current remains discontinuous (the transformer has periods of zero current) providing there is a dead time ( $T_{dt}$ ) between the instant the secondary current reaches zero and the start of the next "on" period. (c and d) If the transformer is loaded beyond this point, some current remains in the transformer at the end of the "off" period and the next "on" period will have a sharp current step at its front end. This step is characteristic of the continuous mode of operation, as the secondary current no longer decays to zero at any part of the conduction period. There is a dramatic change in the transfer function at the point of entering continuous mode, and if the error-amplifier bandwidth has not been drastically reduced, the circuit will oscillate.

#### 4.4 Discontinuous-Mode Operation

Figure 4.1 shows a master output and one slave output. As in all other topologies shown previously, a negative-feedback loop will be closed around the master output  $V_{om}$ . A fraction of  $V_{om}$  will be compared to a reference, and the error signal will control the “on” time of Q1 (the pulse width), so as to regulate the sampled output voltage equal to the reference voltage against line and load changes. Hence, the master output is fully regulated. However, the slaves will also be well regulated against line changes and somewhat less well against load changes because the secondary winding voltages tend to track the master voltage. As a result, the slave line and load regulation is better than for the previously discussed forward-type topologies.

During the Q1 “on” time, there is a fixed voltage across  $N_p$  and current in it ramps up linearly (Figure 4.1b) at a rate of  $di/dt = (V_{dc}-1)/L_p$ , where  $L_p$  is the primary magnetizing inductance. At the end of the “on” time, the primary current has ramped up to  $I_p = (V_{dc}-1)T_{on}/L_p$ . This current represents a stored energy of

$$E = \frac{L_p(I_p)^2}{2} \quad (4.1)$$

where  $E$  is in joules  
 $L_p$  is in henries  
 $I_p$  is in amperes

Now when Q1 turns “off,” the current in the magnetizing inductance forces a reversal of polarities on all windings. (This is called *fly-back action*.) Assume, for the moment, that there are no slave windings and only the master secondary  $N_m$ . Since the current in an inductor cannot change instantaneously, at the instant of turn “off,” the primary current transfers to the secondary at an amplitude  $I_s = I_p(N_p/N_m)$ .

After a number of cycles, the secondary DC voltage has built up to a magnitude (calculated below) of  $V_{om}$ . Now with Q1 “off,” the dot end of  $N_m$  is positive with respect to its no-dot end and current flows out of it, but ramps down linearly (Figure 4.1c) at a rate  $dI_s/dt = V_{om}/L_s$ , where  $L_s$  is the secondary inductance. The discontinuous mode action is defined as follows.

If the secondary current has ramped down to zero before the start of the next Q1 “on” time, all the energy stored in the primary when Q1 was “on” has been delivered to the load and the circuit is said to be operating in the discontinuous mode.

Since an amount of energy  $E$  in joules delivered in a time  $T$  in seconds represents input power in watts, we can calculate the input

## 124 Switching Power Supply Design

power as follows: At the end of one period, power  $P$  drawn from  $V_{dc}$  is

$$P = \frac{1/2 L_p (I_p)^2}{T} W \quad (4.2a)$$

But  $I_p = (V_{dc} - 1)T_{on}/L_p$ . Then

$$P = \frac{[(V_{dc} - 1)T_{on}]^2}{2TL_p} \approx \frac{(V_{dc}T_{on})^2}{2TL_p} W \quad (4.2b)$$

As can be seen from Eq. 4.2b, the feedback loop maintains constant output voltage by keeping the product  $V_{dc}T_{on}$  constant.

### 4.4.1 Relationship Between Output Voltage, Input Voltage, “On” Time, and Output Load

Let us assume an efficiency of 80%, then

$$\begin{aligned} \text{Input power} &= 1.25 (\text{output power}) \\ &= \frac{1.25(V_o)^2}{R_o} = \frac{1/2(L_p I_p^2)}{T} \end{aligned}$$

But  $I_p = V_{dc}T_{on}/L_p$  since maximum “on” time  $T_{on}$  occurs at minimum supply voltage  $V_{dc}$ , as can be seen from Eq. 4.2b.

Then  $1.25(V_o)^2/R_o = 1/2 L_p V_{dc}^2 T_{on}^2 / L_p^2 T$  or

$$V_o = V_{dc}T_{on} \sqrt{\frac{R_o}{2.5TL_p}} \quad (4.3)$$

Thus the feedback loop will regulate the output by decreasing  $T_{on}$  as  $V_{dc}$  or  $R_o$  goes up, increasing  $T_{on}$  as  $V_{dc}R_o$  goes down.

### 4.4.2 Discontinuous-Mode to Continuous-Mode Transition

In Figures 4.2a and 4.2b the solid lines represent primary and secondary currents in the discontinuous mode. Primary current is a triangle starting from zero and rising to a level  $I_{p1}$  (point B) at the end of the power transistor “on” time.

At the instant of Q1 turn “off,” the current  $I_{p1}$  established in the primary winding is transferred to the secondary so as to maintain the ampere-turns ratio. This current is dumped into the secondary capacitors and load during the “off” period. The secondary current ramps downward at a rate  $dI_s/dt = (V_o + 1)/L_s$ , where  $L_s$  is the secondary

inductance, which is  $(N_s/N_p)^2$  times the primary magnetizing inductance. This current reaches zero at time  $I$ , leaving a dead time  $T_{dt}$  before the start of the next turn “on” period at point  $F$ . All the current and hence energy stored in the primary during the previous “on” period has now been completely delivered to the load before the next turn “on.” The average DC output current will be the average of the triangle  $GHI$  multiplied by its duty cycle of  $T_{off}/T$ .

Now, to remain in the discontinuous mode, there must be a dead time  $T_{dt}$  (Figure 4.2b) between the time the secondary current has dropped to zero and the start of the next power transistor “on” time. As more power is demanded (by decreasing  $R_o$ ),  $T_{on}$  must increase to keep output voltage constant (see Eq. 4.3). As  $T_{on}$  increases (at constant  $V_{dc}$ ), primary current slope remains constant and the peak current rises from  $B$  to  $D$  as shown in Figure 4.2a. Secondary peak current ( $= I_p N_p/N_s$ ) increases from  $H$  to  $K$  in Figure 4.2b and starts later in time (from  $G$  to  $J$ ).

Since the output voltage is kept constant by the feedback loop, the secondary slope  $V_o/L_s$  remains constant and the point at which the secondary current falls to zero moves closer to the start of the next turn “on.” This reduces  $T_{dt}$  until a point  $L$  is reached where the secondary current has just fallen to zero at the instant of the next turn “on.” This load current marks the end of the discontinuous mode. Notice that if the supply voltage falls, the “on” time  $T_{on}$  must increase as  $V_{dc}$  decreases to maintain constant output voltage and this will have the same effect.

Notice that as long as the circuit is in the discontinuous mode so that a dead time always remains, increasing the “on” time increases the area of the primary and secondary current triangle  $GHI$  up to the limit of the area  $JKL$ . Further, since the DC output current is the average of the secondary current triangle multiplied by its duty cycle, then during the very next “off” period following an increase in “on” time, more secondary current is immediately available to the load.

When the dead time has been lost, however, any further increase in load current demand will increase the “on” time and decrease the “off” time as the back end of the secondary current can no longer move to the right. The secondary current will start later than point  $J$  (Figure 4.2b) and from a higher point than  $K$ . Then at the start of the next “on” period (position  $F$  in Figure 4.2a or  $L$  in Figure 4.2b), there is still some current or energy left in the transformer.

Now the front end of the primary current will have a small step. The feedback loop tries to deliver the increased DC load current demand by keeping the “on” time later than point  $J$ . Now at each successive “off” time, the current remaining at the end of the “off” time and hence the current step at the start of the next “on” time increase.

## 126 Switching Power Supply Design

Finally after many switching cycles, the front-end step of primary current and the back-end current at the end of the “off” time in Figure 4.2d are sufficiently high so that the area XYZW is somewhat larger than that sufficient to supply the output load current. Now the feedback loop starts to decrease the “on” time so that the primary trapezoid lasts from  $M$  to  $P$  and the secondary current trapezoid lasts from  $T$  to  $W$  (Figures 4.2a and 4.2b).

At this point, the volt-seconds across the transformer primary when the power transistor is “on” is equal to the “off” volt-seconds across it when the transistor is “off.” For this condition, the transformer core is always reset to its original point on the hysteresis loop at the end of a full cycle. It is also the condition where the average or DC voltage across the primary is zero. This is an essential requirement, since the DC resistance in the primary is near zero and it is not possible to support a long-term DC voltage across zero resistance.

Once the continuous mode has been established, increased load current is supplied initially by an increase in “on” time (from  $MP$  to  $MS$  in Figure 4.2c). For fixed-frequency operation this results in a decrease in “off” time from  $TW$  to  $XW$  (Figure 4.2d) as the back end of the secondary current pulse cannot move further to the right in time because the dead time has vanished. Although the peak of the secondary current has increased somewhat (from point  $U$  to  $Y$ ), the area lost in the decreased “off” time ( $T$  to  $X$ ) is greater than the area gained in the slope change from  $UV$  to  $YZ$  in Figure 4.2d.

Thus, in the continuous mode, a sudden increase in DC output current initially causes a decrease in width and a smaller increase in height of the secondary current trapezoid. After many switching cycles, the average trapezoid height builds up and the width relaxes back to the point where the “on” volt-seconds again equals the “off” volt-seconds across the primary.

In addition, since the DC output voltage is proportional to the area of the secondary current trapezoid, the feedback loop, in attempting to keep the output voltage constant against an increased current demand, first drastically decreases the output voltage and then, after many switching cycles, corrects it by building up the amplitude of the secondary current trapezoid. This is the physical-circuits significance of the so-called right-half-plane-zero, which forces the drastic reduction in error-amplifier bandwidth to stabilize the feedback loop. The right-half-plane-zero will be discussed further in the chapter on loop stabilization.

**After Pressman** *In a fixed-frequency system, the immediate effect of increasing the “on” period (to increase primary and hence output current) will be to decrease the “off” period (the period for transfer of current to the output). Since the inductance of the transformer prevents rapid changes*

*in current, the immediate effect of trying to increase current is to cause a short-term decrease in output current. (This is a transitory  $180^\circ$  phase shift between cause and effect). This short transitory phase shift is the cause of the right-half-plane-zero in the transfer function. It is a non-compensatable dynamic effect and forces the designer to provide a very low-frequency roll off in the control loop to maintain stability. Hence transient performance will not be good. The flyback converter in the continuous mode has a boost-like converter characteristic and any converter or combination of converters that have a boost-type characteristic will have the right-half-plane-zero problem. ~K.B.*

#### 4.4.3 Continuous-Mode Flyback— Basic Operation

The flyback topology is widely used for high output voltages at relatively low power ( $\leq 5000$  V at  $< 15$  W). It can also be used at powers of up to 150 W if DC supply voltages are high enough ( $\geq 160$  V) so that primary currents are not excessive. The feature which makes it valuable for high output voltages is that it requires no output inductor. In forward converters, discussed above, output inductors become a troublesome problem at high output voltages because of the large voltages they have to sustain. Not requiring a high voltage free-wheeling diode is also a plus for the flyback in high voltage supplies.

**After Pressman** *A further advantage for high voltage applications is that relatively large voltages can be obtained with relatively fewer transformer turns. ~K.B.*

The flyback topology is attractive for multiple output supplies because the output voltages track one another for line and load changes, far better than they do in the forward-type converters described earlier. The absence of output inductors results in better tracking. As a result, flybacks are a frequent choice for supplies with many output voltages (up to 10 isolated outputs are not uncommon). The power can be in the range of 50 to 150 W.

Although they can be used from DC input voltages as low as 5 V, it is more usual to find them used for the usual rectified 160 VDC obtained from a 115-V AC power line input. By careful design of the turns ratios, they can also be used in universal line input applications ranging from the rectified output of 160 volts DC from 110 AC inputs up to the 320 V DC obtained from a 220-V AC power line, without the need for the voltage doubling—full-wave rectifying scheme (switch S1) shown in Figure 3.1.

The latter scheme, although very widely used, has the objectionable feature that to do the switching from 115 to 220 V AC, both ends of

## 128 Switching Power Supply Design

the switch in Figure 3.1 have to be accessible on the outside of the supply, which is a safety hazard. Or the supply must be opened to change the switch position. Both these alternatives have drawbacks. An alternative scheme not requiring switching will be discussed in Section 4.3.5.

Both modes have an identical circuit diagram, shown in Figure 4.1, and it is only the transformer's magnetizing inductance and output load current that determines the operating mode. It has been shown that with a given magnetizing inductance, a circuit that has been designed for the discontinuous mode will move into the continuous mode when the output load current is increased beyond a unique boundary. The mechanism for this and its consequence are discussed in more detail below.

The discontinuous mode (as shown in Figure 4.2*a*) does not have a front-end step in the primary current. At turn "off" (as shown in Figure 4.2*b*), the secondary current will be a decaying triangle that has ramped down to zero before the next turn "on." All the energy stored in the primary during the "on" period has been completely delivered to the secondary and thus to the load before the next turn "on."

In the continuous mode, however (as seen in Figure 4.2*c*), the primary current does have a front-end step and the characteristic of a rising current ramp following the step. During the "off" period of Q1 (Figure 4.2*d*), the secondary current has the shape of a decaying triangle sitting on a step with current still remaining in the secondary at the instant of the next turn "on" action. Clearly there is still some energy left in the transformer at the instant of the next turn "on."

The two modes have significantly different operating properties and usages. The discontinuous mode, which does not have a right-half-plane-zero in the transfer function, responds more rapidly to transient load changes with a lower transient output voltage spike.

A penalty is paid for this performance, in that the secondary peak current in the discontinuous mode can be between two and three times greater than that in the continuous mode. This is shown in Figures 4.2*b* and 4.2*d*. Secondary DC load current is the average of the current waveshapes in those figures. Also, assuming closely equal "off" times, it is obvious that the triangle in the discontinuous mode must have a much larger peak than the trapezoid of the continuous mode for the two waveshapes to have equal average values.

With larger peak secondary currents, the discontinuous mode has a larger transient output voltage spike at the instant of turn "off" (Section 4.3.4.1) and requires a larger LC spike filter to remove it.



Also, the larger secondary peak current at the start of turn “off” in the discontinuous mode causes a greater RFI problem. Even for moderate output powers, the very large initial spike of secondary current at the instant of turn “off” causes a much more severe noise spike on the output ground bus, because of the large  $di/dt$  into the output bus inductance.

**After Pressman** *A major advantage of the discontinuous mode is that the secondary rectifier diodes turn “off” under low current stress conditions. Also they are fully “off” before the next “on” edge of Q1. Hence the problem of diode reverse recovery is eliminated. This is a major advantage in high voltage applications as diode reverse recovery current spikes are difficult to eliminate and are a rich source of RFI. ~K.B.*

Due to the poor form factor, secondary RMS currents in the discontinuous mode can be much larger than those in the continuous mode. Hence, the discontinuous mode requires larger secondary wire size and output filter capacitors with larger ripple current ratings. The rectifier diodes will also run hotter in the discontinuous mode because of the larger secondary RMS currents. Further, the primary peak currents in the discontinuous mode are larger than those in the continuous mode. For the same output power, the triangle of Figure 4.2a must have a larger peak than the trapezoid of Figure 4.2c. The consequence is that the discontinuous mode with its larger peak primary current requires a power transistor of higher current rating and possibly higher cost. Also, the higher primary current at the turn “off” edge of Q1 results in a potential for greater RFI problems.

Despite all the disadvantages of the discontinuous mode, it is much more widely used than the continuous mode. This is so for two reasons. First, as mentioned above, the discontinuous mode, with an inherently smaller transformer magnetizing inductance, responds more quickly and with a lower transient output voltage spike to rapid changes in output load current or input voltage. Second, because of a unique characteristic of the continuous mode (its transfer function has a right-half-plane-zero, to be discussed in a later chapter on feedback loop stabilization), the error amplifier bandwidth must be drastically reduced to stabilize the feedback loop.

**After Pressman** *Modern power devices, such as the Power Integration’s Top Switch range of products, have the “noisy” FET drain part of the chip isolated from the heat sink tab. This, together with integrated drive and control circuits, which further reduce radiating area, very much reduces the RFI problems normally associated with the discontinuous flyback topology. ~K.B.*



## 4.5 Design Relations and Sequential Design Steps

### 4.5.1 Step 1: Establish the Primary/Secondary Turns Ratio

For the most expedient design, there are a number of decisions that should be made in the following logical sequence.

First select a core size to meet the power requirements.

Next choose the primary/master secondary turns ratio  $N_p/N_{sm}$  to determine the maximum “off”-voltage stress  $\overline{V_{ms}}$  on the power transistor in the absence of a leakage inductance spike as follows:

Neglecting the leakage spike, the maximum transistor voltage stress at maximum DC input  $\overline{V_{dc}}$  and for a 1-V rectifier drop is

$$\overline{V_{ms}} = \overline{V_{dc}} + \frac{N_p}{N_{sm}}(V_o + 1) \quad (4.4)$$

where  $\overline{V_{ms}}$  is chosen sufficiently low so that a leakage inductance spike of  $0.3V_{dc}$  on top of that still leaves a safety margin of about 30% below the maximum pertinent transistor rating ( $V_{ceo}$ ,  $V_{cer}$ , or  $V_{cev}$ ).

### 4.5.2 Step 2: Ensure the Core Does Not Saturate and the Mode Remains Discontinuous

To ensure that the core does not drift up or down its hysteresis loop, the “on” volt-second product ( $A1$  in Figure 4.1d) must equal the reset volt-second product ( $A2$  in Figure 4.1d). Assume that the “on” drop of  $Q1$  and the forward drop of the rectifier  $D2$  are both 1 V:

$$(\overline{V_{dc}} - 1)\overline{T_{on}} = (V_o + 1) \frac{N_p}{N_{sm}} T_r \quad (4.5)$$

where  $T_r$  shown in Figure 4.1c is the reset time required for the secondary current to return to zero.

To ensure the circuit operates in the discontinuous mode, a dead time ( $T_{dt}$  in Figure 4.1c) is established so that the maximum “on” time  $\overline{T_{on}}$ , which occurs when  $V_{dc}$  is a minimum, plus the reset time  $T_r$  is only 80% of a full period. This leaves 0.2T margin against unexpected decreases in  $R_o$ , which according to Eq. 4.3 would force the feedback loop to increase  $T_{on}$  in order to keep  $V_o$  constant.

As for the boost regulator, which is also a flyback type (Sections 1.4.2 and 1.4.3), it was pointed out that if the error amplifier has been designed to keep the loop stable only in the discontinuous mode, it may break into oscillation if the circuit momentarily enters the continuous mode.

Increasing DC load current or decreasing  $V_{dc}$  causes the error amplifier to increase  $T_{on}$  in order to keep  $V_o$  constant (Eq. 4.3). This increased  $T_{on}$  eats into the dead time  $T_{dt}$ , and eventually the secondary current does not fall to zero by the start of the next Q1 “on” time. This is the start of the continuous mode, and if the error amplifier has not been designed with a drastically lower bandwidth than required for discontinuous mode, the circuit will oscillate. To ensure that the circuit remains discontinuous, the maximum “on” time that will generate the desired maximum output power is established:

$$\overline{T_{on}} + T_r + T_{dt} = T$$

or

$$\overline{T_{on}} + T_r = 0.8T \quad (4.6)$$

Now in Eqs. 4.5 and 4.6, there are two unknowns, as  $N_p/N_{sm}$  has been calculated from Eq. 4.4 for specified  $\overline{V_{dc}}$  and  $\overline{V_{ms}}$ . Then from the last two relations

$$\overline{T_{on}} = \frac{(V_o + 1)(N_p/N_{sm})(0.8T)}{(\overline{V_{dc}} - 1) + (V_o + 1)(N_p/N_{sm})} \quad (4.7)$$

#### 4.5.3 Step 3: Adjust the Primary Inductance Versus Minimum Output Resistance and DC Input Voltage

From Eq. 4.3, the primary inductance is

$$L_p = \frac{R_o}{2.5T} \left( \frac{V_{dc}\overline{T_{on}}}{V_o} \right)^2 = \frac{(V_{dc}\overline{T_{on}})^2}{2.5T\overline{P_o}} \quad (4.8)$$

#### 4.5.4 Step 4: Check Transistor Peak Current and Maximum Voltage Stress

If the transistor is a bipolar type, it must have an acceptably high gain at the peak current operating current  $I_p$ . This is

$$I_p = \frac{V_{dc}\overline{T_{on}}}{L_p} \quad (4.9)$$

where  $\overline{V_{dc}}$  is specified and  $\overline{T_{on}}$  is calculated from Eq. 4.7 and  $L_p$  is calculated from Eq. 4.8.

If Q1 is a MOSFET, it should have a peak current rating about 5 to 10 times the value calculated from Eq. 4.9 so that its “on”-state resistance is low enough to yield an acceptably low voltage drop and power loss.

## 132 Switching Power Supply Design

### 4.5.5 Step 5: Check Primary RMS Current and Establish Wire Size

The primary current is a triangle of peak amplitude  $I_p$  (Eq. 4.9) at a maximum duration  $\overline{T_{on}}$  out of every period  $T$ . Its RMS value (Section 2.2.10.6) is

$$I_{\text{rms(primary)}} = \frac{I_p}{\sqrt{3}} \sqrt{\frac{\overline{T_{on}}}{T}} \quad (4.10)$$

where  $I_p$  and  $\overline{T_{on}}$  are as given by Eqs. 4.9 and 4.7.

At 500 circular mils per RMS ampere, the required number of circular mils is

$$\begin{aligned} \text{Circular mils required (primary)} &= 500 I_{\text{rms(primary)}} \\ &= 500 \frac{I_p}{\sqrt{3}} \sqrt{\frac{\overline{T_{on}}}{T}} \end{aligned} \quad (4.11)$$

### 4.5.6 Step 6: Check Secondary RMS Current and Select Wire Size

The secondary current is a triangle of peak amplitude  $I_s = I_p(N_p/N_s)$  and duration  $T_r$ . Primary/secondary turns ratio  $N_p/N_s$  is given by Eq. 4.4 and  $T_r = (T - T_{on})$ . Secondary RMS current is then

$$I_{\text{rms(secondary)}} = \frac{I_p(N_p/N_s)}{\sqrt{3}} \sqrt{\frac{T_r}{T}} \quad (4.12)$$

At 500 circular mils per RMS ampere, the required number of circular mils is

$$\text{Secondary circular mils required} = 500 I_{\text{rms(secondary)}} \quad (4.13)$$

## 4.6 Design Example for a Discontinuous-Mode Flyback Converter

We will now look at a worked design example for a flyback converter with the following specifications:

$V_o$	5.0 V
$P_o(\text{max})$	50 W
$I_o(\text{max})$	10 A
$I_o(\text{min})$	1.0 A
$V_{\text{dc}}(\text{max})$	60 V
$V_{\text{dc}}(\text{min})$	38 V
Switching frequency	50 kHz

First, select the voltage rating of the transistor as this mainly determines the transformer turns ratio. Choose a device with a 200-V rating. In Eq. 4.4 choose the maximum stress  $V_{ms}$  on the transistor in the “off” state (excluding the leakage inductance spike) as 120 V. Then even with a 25% or 30-V leakage spike, this leaves a 50-V margin to the maximum voltage rating. Then from Eq. 4.4

$$120 = 60 + \frac{N_p}{N_{sm}}(V_o + 1) \quad \text{or} \quad \frac{N_p}{N_{sm}} = 10$$

Now choose maximum “on” time from Eq. 4.7:

$$\begin{aligned} \overline{T_{on}} &= \frac{(V_o + 1)(N_p/N_{sm})(0.8T)}{(V_{dc} - 1) + (V_o + 1)N_p/N_{sm}} \\ &= \frac{6 \times 10 \times 0.8 \times 20}{(38 - 1) + 6 \times 10} \\ &= 9.9 \mu\text{s} \end{aligned}$$

From Eq. 4.8

$$\begin{aligned} L_p &= \frac{(V_{dc}\overline{T_{on}})^2}{2.5T P_o} \\ &= \frac{(38 \times 9.9 \times 10^{-6})^2}{2.5 \times 20 \times 10^{-6} \times 50} \\ &= 56.6 \mu\text{H} \end{aligned}$$

From Eq. 4.9

$$\begin{aligned} I_p &= \frac{V_{dc}\overline{T_{on}}}{L_p} \\ &= \frac{38 \times 9.9 \times 10^{-6}}{56.6 \times 10^{-6}} \\ &= 6.6 \text{ A} \end{aligned}$$

From Eq. 4.10, primary RMS current is

$$\begin{aligned} I_{\text{rms(primary)}} &= \frac{I_p}{\sqrt{3}} \sqrt{\frac{\overline{T_{on}}}{T}} \\ &= \frac{6.6}{\sqrt{3}} \times \sqrt{\frac{9.9}{20}} \\ &= 2.7 \text{ A} \end{aligned}$$

## 134 Switching Power Supply Design

From Eq. 4.11, primary circular mils requirement is

$$I_{(\text{primary circular mils})} = 500 \times 2.7 = 1350 \text{ circular mils}$$

This calls for a No. 19 wire of 1290 circular mils, which is close enough.

From Eq. 4.12, secondary RMS current is

$$I_{\text{rms}(\text{secondary})} = \frac{I_p(N_p/N_s)}{\sqrt{3}} \sqrt{\frac{T_r}{T}}$$

But reset time  $T_r$  is

$$(0.8T - \overline{T_{\text{on}}}) = (16 - 9.9) = 6.1 \mu\text{s}$$

Then

$$\begin{aligned} I_{\text{rms}(\text{secondary})} &= \frac{6.6 \times 10}{\sqrt{3}} \sqrt{\frac{6.1}{20}} \\ &= 21 \text{ A} \end{aligned}$$

We see that from Eq. 4.12, the required number of circular mils is  $500 \times 21 = 10,500$ . This calls for No. 10 wire, which is impractically large in diameter. A foil winding or a number of smaller diameter wires in parallel with an equal total circular-mil area would be used.

**After Pressman** *Contrary to popular belief, the wire size and leakage inductance in a flyback transformer are important design parameters. Multiple strands of wire in parallel are required, with the maximum wire size selected to minimize skin and proximity effects. Even though the secondary energy comes from the energy stored in the transformer core, leakage inductance must still be minimized to ensure good energy transfer from the primary winding to the secondary windings to reduce voltage spikes on Q1 at the "off" transition. This will reduce the amount of snubbing required on Q1 and reduce RFI. (See Chapter 7.) ~K.B.*

The output capacitor is chosen on the basis of specified peak-to-peak output voltage ripple as follows:

At maximum output current, the filter capacitor  $C_o$  carries the 10-A output current for all but the  $6.1 \mu\text{s}$  reset period, or  $13.9 \mu\text{s}$ . The voltage on this capacitor droops by  $V = I(T - t_{\text{off}})/C_o$ . Then for a voltage droop of 0.05 V

$$\begin{aligned} C_o &= \frac{10 \times 13.9 \times 10^{-6}}{0.05} \\ &= 2800 \mu\text{F} \end{aligned}$$

From Section 1.4.7, the average ESR of a 2800- $\mu\text{F}$  aluminum electrolytic capacitor is

$$R_{\text{esr}} = 65 \times 10^{-6} / C_o = 0.023 \, \Omega$$

At the instant of transistor turn “off,” a peak secondary current of 66 amps flows through the above capacitor ESR, causing a thin spike of  $66 \times 0.023 = 1.5 \text{ V}$ . This large-amplitude thin spike at transistor turn “off” is a universal problem with flybacks having a large  $N_p/N_s$  ratio. It is usually solved by using a larger filter capacitor than calculated as above (since  $R_{\text{esr}}$  is inversely proportional to  $C_o$ ) and/or integrating away the thin spike with a small LC circuit.

**After Pressman** *Since the spike contains a large amount of high frequency components, combining several capacitors in parallel will reduce the spike amplitude significantly. Small ceramic and film caps are often used.*  
~K.B.

Selecting a transformer core for a flyback topology circuit is significantly different than selecting for a forward converter. Remember in the flyback that when current flows in the primary, the secondary current is zero, and there is no current flow in the secondary to buck out the primary ampere turns as there is in the forward converters. Thus in the flyback, all the primary ampere turns tend to saturate the core.

In contrast, in non-flyback topologies, secondary load current flows when primary current flows and is in the direction (by Lenz’s law) to cancel the ampere turns of the primary. It is only the primary magnetizing current that drives the core over its hysteresis loop and moves it toward saturation. That magnetizing current is kept a small fraction of the primary load current by providing a large magnetizing inductance and hence core saturation is not a basic a problem with non-flyback topologies.

Hence, flyback transformer cores must have some means of carrying large primary currents without saturating. This is done by choosing low permeability materials such as MPP (molybdenum permalloy powder) cores that have an inherent air gap or by using gapped ferrite cores (Section 2.3.9.3 and Chapter 7). This is discussed further in the following section.

#### 4.6.1 Flyback Magnetics

Referring to Figure 4.1a, it is seen from the winding dots that when the transistor is “on” and current flows in the primary, no secondary currents flow. This is totally different from forward-type converters,

## 136 Switching Power Supply Design

in which current flows in the secondary when it flows in the primary. Thus in a forward-type converter, primary current flows into a dot end and secondary current flows out of a dot end.

Primary and secondary load ampere-turns then cancel each other out and do not move the core across its hysteresis loop. In the forward-type converters, it is only the magnetizing current that drives the core across the hysteresis loop and may potentially saturate it. But this magnetizing current is a small fraction (rarely  $>10\%$ ) of the total primary current.

In a flyback converter, however, the entire triangle of primary current shown in Figure 4.1*b* drives the core across the hysteresis loop as it is not canceled out by any secondary ampere turns. Thus, even at very low output power, an ungapped ferrite core would almost immediately saturate and destroy the transistor if nothing were done to prevent it.

To prevent core saturation in the flyback transformer, the core is gapped. The gapped core can be either of two types. It can be a solid ferrite core with a known air-gap length obtained by grinding down the center leg in EE or cup-type cores. The known gap length can also be obtained by inserting plastic shims between the two halves of an EE, cup, or UU core.

A more usual gapped core for flyback converters is the MPP or molypermalloy powder core. Such cores are made of a baked and hardened mix of magnetic powdered particles. These powdered particles are mixed in a slurry with a plastic resin binder and cast in the shape of a toroid. Each magnetic particle in the toroid is thus encapsulated within a resin envelope that behaves as a “distributed air gap” and acts to keep the core from saturating. The basic magnetic material that is ground up into a powder is Square Permalloy 80, an alloy of 79% nickel, 17% iron, and 4% molybdenum, made by Magnetics Inc. and Arnold Magnetics, among others.

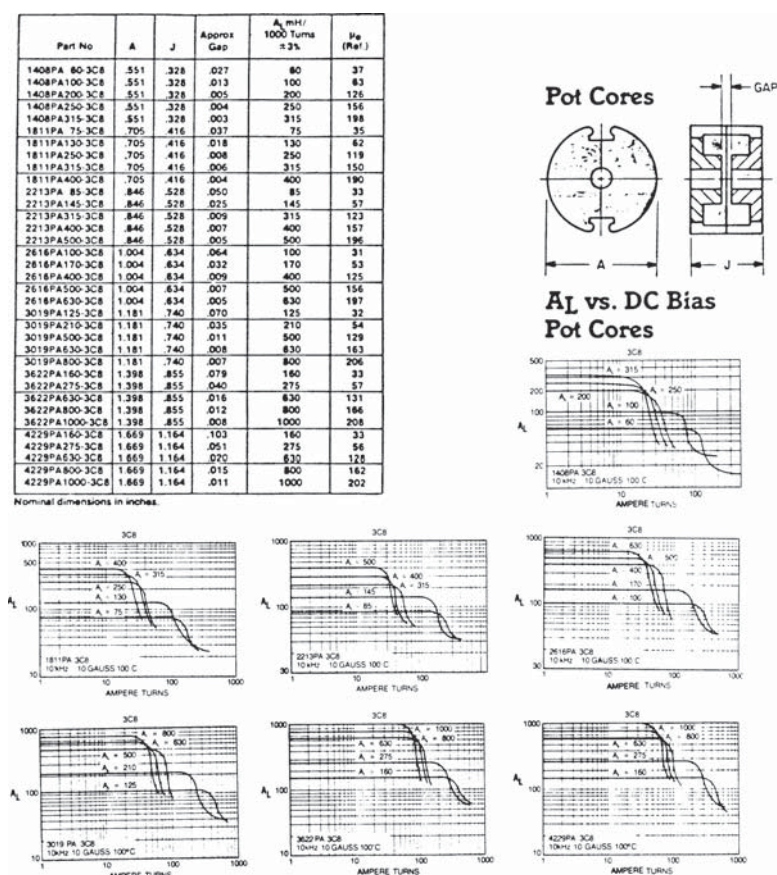
The permeability of the resulting toroid is determined by controlling the concentration of magnetic particles in the slurry. Permeabilities are controlled to within  $\pm 5\%$  over large temperature ranges and are available in discrete steps ranging from 14 to 550. Toroids with low permeability behave like gapped cores with large air gaps. They require a relatively large number of turns to yield a desired inductance but tolerate many ampere-turns before they saturate. Higher permeability cores require relatively fewer turns but saturate at a lower number of ampere-turns.

Such MPP cores are used not only for flyback transformers in which all the primary current is DC bias current. They are also used for forward converter output inductors where, as has been seen, a unique inductance is required at the large DC output current bias (Section 1.3.6).

#### 4.6.2 Gapping Ferrite Cores to Avoid Saturation

Adding an air gap to a solid ferrite core achieves two results. First, it tilts the hysteresis loop as shown in Figure 2.5 and hence decreases its permeability, which must be known to select the number of turns for a desired inductance. Second, and more important, it increases the number of ampere turns it can tolerate before it saturates.

Core manufacturers often offer curves that permit calculation of the number of turns for a desired inductance and the number of ampere-turns at which saturation commences. Such curves are shown in Figure 4.3 and show  $A_{lg}$ , the inductance per 1000 turns with an air



**FIGURE 4.3** Inductance per 1000 turns ( $A_{lg}$ ) for various ferrite cores with various air gaps. Note the “cliff” points in ampere-turns where saturation commences. (Courtesy Ferroxcube Corporation.)



## 138 Switching Power Supply Design

gap and the number of ampere-turns ( $NI_{\text{sat}}$ ) where saturation starts to set in. Since inductance is proportional to the square of the number of turns, the number of turns  $N_l$  for any inductance  $L$  is calculated from

$$N_l = 1000 \sqrt{\frac{L}{A_{lg}}} \quad (4.14)$$

Figure 4.3 shows  $A_{lg}$  curves for a number of different air gaps and the “cliff” point at which saturation starts. It can be seen that the larger the air gap, the lower the value of  $A_{lg}$  and the larger the number of ampere-turns at which saturation starts. If such curves were available for all cores at various air gaps, Eq. 4.14 would give the number of turns for any selected air gap from the value of  $A_{lg}$  read from the curve. The cliff point on the curve would tell whether, at those turns and for the specified primary current, the core had fallen over the saturation cliff.

Such curves, though, are not available for all cores and all air gaps. This is no problem, because  $A_{lg}$  can be calculated with reasonable accuracy from Eq. 2.39 using  $A_l$  with no gap, which is always given in the manufacturers’ catalogs. The cliff point at which saturation starts can be calculated from Eq. 2.37 for any air gap. The cliff point corresponds to the flux density in iron  $B_i$ , where the core material itself starts bending over into saturation.

From Figure 2.3, it is seen that this is not a very sharp breaking point, but occurs around 2500 G for this ferrite material (Ferroxcube 3C8). Thus the cliff in ampere-turns is found by substituting 2500 G in Eq. 2.37. As noted in connection with Eq. 2.37, in the usual case, the air-gap length  $l_a$  is much larger than  $l_i/u$  as  $u$  is so large. Then the iron flux density as given by Eq. 2.37 is determined mainly by the air-gap length  $l_a$ .

### 4.6.3 Using Powdered Permalloy (MPP) Cores to Avoid Saturation

These toroidal cores are widely used and made by Magnetics Inc. (data in catalog MPP303S) and by Arnold Co. (data in catalog PC104G).

**After Pressman** *The term transformer in the phrase flyback transformer is a misnomer and is very misleading. For true transformer action to take place both primary and secondaries must conduct current at the same time. We are all aware that a true transformer conserves the primary to secondary voltage ratio (irrespective of current). In the flyback case the so-called transformer conserves the primary to secondary ampere-turns ratio (irrespective of voltage). This means it is really a “choke”—an inductor with a DC component of current and additional windings. I find it much easier and less confusing to design my flyback “transformers” from this perspective. The reader may also find it helpful to use this approach because the inductance*

becomes the dependant variable and can be easily adjusted to get the desired results. Chapter 7 deals with the design in this way.

You will see from the following that although he does not mention it, Pressman is leading you in the direction of choke design. ~K.B.

The problem in designing a core of desired inductance at a specified maximum DC current bias is to select a core geometry and material permeability, such that the core does not saturate at the maximum ampere-turns to which it is subjected. There are a limited number of core geometries, each available in permeabilities ranging from 14 to 550. Selection procedures are described in the catalogs mentioned above, but the following has been found more direct and useful.

In the Magnetics Inc. catalog, one full page (Figure 4.4) is devoted to each size toroid, and for each size, its  $A_l$  value (inductance in millihenries per 1000 turns) is given for each discrete permeability. Figure 4.5, also from the Magnetics Inc. catalog, gives the falloff in permeability (or  $A_l$  value) for increasing magnetizing force in oersteds for core materials of the various available permeabilities. (Recall the oersted-ampere-turns relation in Eq. 2.6.)

A core geometry and permeability can be selected so that at the maximum DC current and the selected number of turns, the  $A_l$  and hence inductance has fallen off by any desired percentage given in Figure 4.5. Then at zero DC current, the inductance will be greater by that percentage. Such inductors or chokes are referred to as “swing-chokes” and in many applications are desirable. For example, if an inductor is permitted to swing a great deal, in an output filter, it can tolerate a very low minimum DC current before it goes discontinuous (Section 1.3.6). But this greatly complicates the feedback-loop stability design and, most often, the inductor in an output filter or transformer in a flyback will not be permitted to “swing” or vary very much between its zero and maximum current value.

Referring to Figure 4.4, it is seen that a core of this specific size is available in permeabilities ranging from 14 to 550. Cores with permeability above 125 have large values of  $A_l$  and hence require fewer turns for a specified inductance at zero DC current bias. But in Figure 4.5 it is seen that the higher-permeability cores saturate at increasingly lower ampere-turns of bias. Hence in power supply usage, where DC current biases are rarely under 1 A, cores of permeability greater than 125 are rarely used, and an inductance swing or change of 10% from zero to the maximum specified current is most often acceptable.

In Figure 4.5, it is seen that for a permeability dropoff or swing of 10%, core materials of permeabilities 14, 26, 60, and 125 can sustain maximum magnetizing forces of only 170, 95, 39, and 19 Oe, respectively. These maximum magnetizing forces in oersteds can be translated into maximum ampere-turns by Eq. 2.6 ( $\overline{H} = 0.4\pi(\overline{NI})/l_m$ ), in

## 140 Switching Power Supply Design

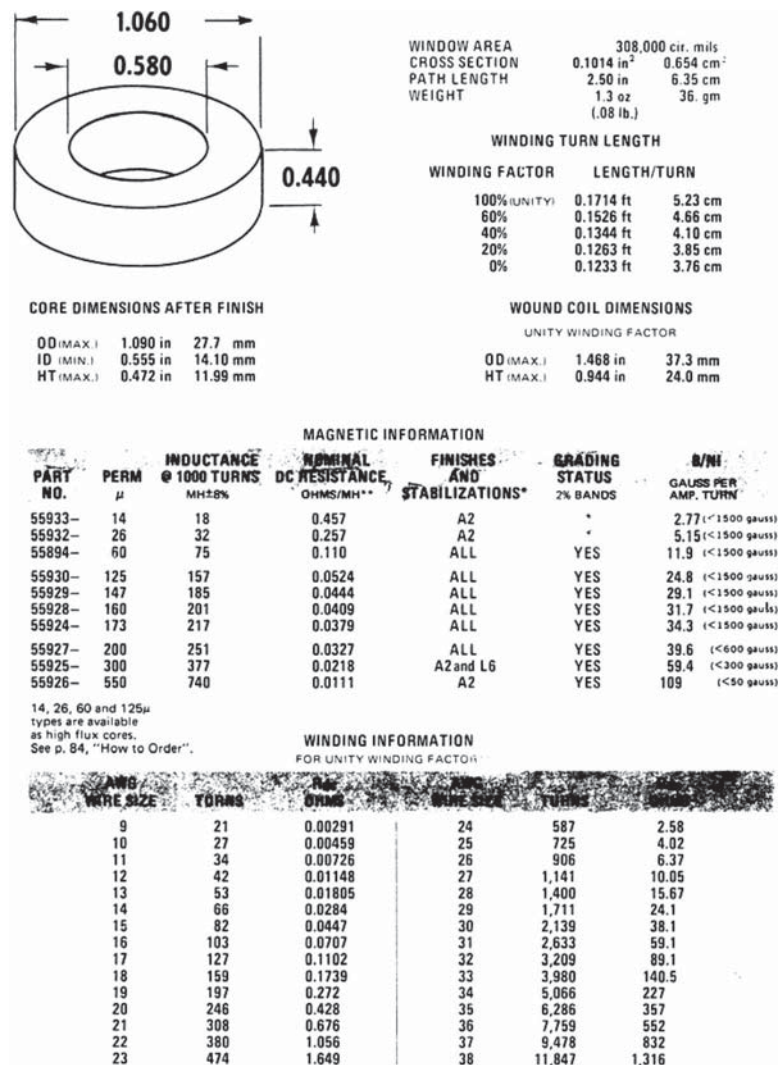


FIGURE 4.4 A typical MPP core. With its large distributed air gap, it can tolerate a large DC current bias without saturating. It is available in a large range of different geometries. (Courtesy Magnetics Inc.)

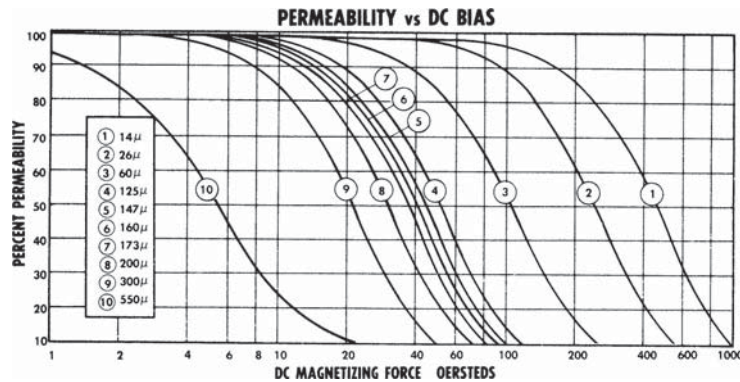


FIGURE 4.5 Falloff in permeability of  $A_1$  for MPP cores of various permeabilities versus DC magnetizing force in oersteds. (Courtesy Magnetics Inc.)

which  $l_m$  is the magnetic path length in centimeters, given in Figure 4.3 for this particular core geometry as 6.35 cm.

From these maximum numbers of ampere-turns ( $\overline{NI}$ ), beyond which inductance falls off more than 10%, the maximum number of turns ( $\overline{N}$ ) is calculated for any peak current. From  $\overline{N}$ , the maximum inductance possible for any core at the specified peak current is calculated as  $L_{\max} = 0.9 A_1 (N_{\max}/1000)^2$ .

Tables 4.1, 4.2, and 4.3 show  $N_{\max}$  and  $L_{\max}$  for three often-used core geometries in permeabilities of 14, 26, 60, and 125 at peak currents of 1, 2, 3, 5, 10, 20, and 50 amperes. These tables permit core geometry and permeability selection at a glance without iterative calculations.

Table 4.1 is used in the following manner. Assume that this particular core has the acceptable geometry. The table is entered horizontally to the first peak current greater than specified value. At that peak current, move down vertically until the first inductance  $L_{\max}$  greater than the desired value is reached. The core at that point is the only one which can yield the desired inductance with only a 10% swing. The number of turns  $N_d$  on that core for a desired inductance  $L_d$  within 5% is given by

$$N_d = 1000 \sqrt{\frac{L_d}{0.95 A_1}}$$

where  $A_1$  is the value in column 3 in Table 4.1. If, moving vertically, no core can be found whose maximum inductance is greater than the desired value, the core with the next larger geometry (greater OD or greater height) must be used.

## 142 Switching Power Supply Design

Magnetics Inc. core number	Perme- ability	$A_l$ , mH per 1000 turns	Maximum $\overline{H}$ for 10% falloff in inductance	$\overline{NI}$ Maximum permissible ampere-turns corresponding to $\overline{H}$	Maximum permissible turns and inductance at those turns for a 10% inductance falloff at indicated peak currents									
					1A	$N_{\max}/L_{\max}$			5A	10A	20A	50A	$I_p$	
						2A	3A							
Core	$\mu$	$A_l$	$H$	$NI$	1A	2A	3A	5A	10A	20A	50A	$I_p$		
55930	125	157	19	96	96 1,382	48 339	32 145	19 56	10 15	5 3.5	2 0.6	$N_{\max}$ $L_{\max}$		
55894	60	75	39	197	197 2,620	99 662	66 294	39 103	20 27	10 7	4 1	$N_{\max}$ $L_{\max}$		
55932	26	32	95	480	480 6,635	240 1,659	160 737	96 265	48 66	24 17	10 3	$N_{\max}$ $L_{\max}$		
55933	14	18	170	859	859 11,954	430 2,995	286 1,325	172 479	86 120	43 30	17 5	$N_{\max}$ $L_{\max}$		

Note: Magnetics Inc. MPP cores. All cores have outer diameter (OD) = 1.060 in, inner diameter (ID) = 0.58 in, height = 0.44 in,  $l_m = 6.35$  cm. All inductances in microhenries.

TABLE 4.1 Maximum number of turns yielding maximum inductance for various peak currents  $I_p$  at maximum inductance falloff of 10% from zero current

Magnetics Inc. core number	Perme- ability	$A_l$ , mH per 1000 turns	Maximum $H$ for 10% falloff in inductance	$\overline{NI}$ Maximum permissible ampere-turns corresponding to $\overline{H}$	Maximum permissible turns and inductance at those turns for a 10% inductance falloff at indicated peak currents									
					1A	$N_{\max}/L_{\max}$			5A	10A	20A	50A	$I_p$	
						2A	3A	4A						
Core	$\mu$	$A_l$	$H$	$NI$	77 363	39 93	26 41	15 14	15 14	8 4	4 1	2 0.24	$N_{\max}$ $L_{\max}$	
55206	125	68	19	77										
55848	60	32	39	158	158 719	79 180	53 81	32 29	32 29	16 7	8 2	3 0.26	$N_{\max}$ $L_{\max}$	
55208	26	14	95	385	385 1,868	193 469	128 206	77 75	77 75	39 19	19 4.5	8 0.8	$N_{\max}$ $L_{\max}$	
55209	14	7.8	170	689	689 3,333	345 836	230 371	138 134	138 134	69 33	34 8	14 1.4	$N_{\max}$ $L_{\max}$	

Note: Magnetics Inc. MPP cores: OD = 0.8 in, ID = 0.5 in, height = 0.25 in,  $l_m = 5.09$  cm. All inductances in microhenries.

**TABLE 4.2** Maximum number of turns and maximum inductance for various peak currents  $I_p$  at a maximum inductance falloff of 10% from zero current

## 144 Switching Power Supply Design

Core	$\mu$	$A_l$	$\overline{H}$	$\overline{NI}$	1A	2A	3A	5A	10A	20A	50A	$I_p$
55438	125	281	19	162	162 6,637	81 1,659	54 737	32 259	16 65	8 16	3 2	$N_{\max}$ $L_{\max}$
55439	60	135	39	333	333 13,473	167 3,389	111 1,497	67 545	33 132	17 35	7 6	$N_{\max}$ $L_{\max}$
55440	26	59	95	812	812 35,011	406 8,753	271 3,900	162 1,394	81 348	41 89	16 14	$N_{\max}$ $L_{\max}$
55441	14	32	170	1454	1,454 60,744	727 15,222	485 6,774	291 2,439	145 605	73 153	29 24	$N_{\max}$ $L_{\max}$

Note: Magnetics Inc. MPP cores: OD = 1.84 in, ID = 0.95 in, height = 0.71 in,  $l_m = 10.74$  in. All inductances in microhenries.

**TABLE 4.3** Maximum number of turns and maximum inductance for various peak currents  $I_p$  at a maximum inductance falloff of 10% from zero current



The core ID must be large enough to accommodate the number of turns of wire selected at the rate of 500 circular mils per RMS ampere, or the next larger size core must be used.

Tables 4.2 and 4.3 show similar data for smaller (OD = 0.80 in) and larger (OD = 1.84 in) families of cores. Similar charts can be generated for all the other available core sizes, but Tables 4.1 to 4.3 bracket about 90% of the possible designs for flyback transformers under 500 W or output inductors of up to 50 A.

A commonly used scheme for correcting the number of turns on a core when an initial selection has resulted in too large an inductance falloff should be noted. If, for an initially selected number of turns and a specified maximum current, the inductance or permeability falloff from Figure 4.5 is down by  $P\%$ , the number of turns is increased by  $P\%$ .

This moves the operating point further out by  $P\%$ , as the magnetizing force in oersteds is proportional to the number of turns. The core slides further down its saturation curve, and it might be thought that the inductance would fall off even more. But since inductance is proportional to the square of the number of turns, and magnetizing force is proportional only to the number of turns, the zero current inductance has been increased by  $2P\%$  and magnetizing force has gone up only by  $P\%$ . The inductance is then correct at the specified maximum current. If the consequent swing is too large, a larger core must be used.

#### 4.6.4 Flyback Disadvantages

Despite its many advantages, the flyback has the following drawbacks.

##### 4.6.4.1 Large Output Voltage Spikes

At the end of the “on” time, the peak primary current is given by Eq. 4.9. Immediately after the end of the “on” time, that primary peak current, multiplied by the turns ratio  $N_p/N_s$ , is driven into the secondary where it decays linearly as shown in Figure 4.1c. In most cases, output voltages are low relative to input voltage, resulting in a large  $N_p/N_s$  ratio and a consequent large secondary current.

At the start of turn “off,” the impedance looking into  $C_o$  is much lower than  $R_o$  (Figure 4.1) and almost all the large secondary current flows into  $C_o$  and its equivalent series resistor  $R_{esr}$ . This produces a large, thin output voltage spike,  $I_p(N_p/N_s)R_{esr}$ . The spike is generally less than 0.5  $\mu$ s in width, as it is differentiated with a time constant of  $R_{esr}C_o$ .

Frequently a power supply specification calls for output voltage ripple only as an RMS or peak-to-peak fundamental value. Such a large, thin spike has a very low RMS value and, if a sufficiently large



## 146 Switching Power Supply Design

output filter capacitor is chosen, the supply can easily meet its RMS ripple specification but can have disastrously high, thin output spikes. It is common to see a 50-mV fundamental peak-to-peak output ripple with a 1-V thin spike sitting on top of it.

Thus, a small  $LC$  filter is almost always added after the main storage capacitor in flybacks. The  $L$  and  $C$  can be quite small as they have to filter out a spike generally less than  $0.5\text{ }\mu\text{s}$  in width. The inductor is usually considerably smaller than the inductor in forward-type converters, but it still has to be stocked, and board space must be provided for it. Output voltage sensing for the error amplifier is taken before this  $LC$  filter.

### 4.6.4.2 Large Output Filter Capacitor and High Ripple Current Requirement

A filter capacitor for a flyback must be much larger than for a forward-type converter. In a forward converter, when the power transistor turns “off” (Figure 2.10), load current is supplied from the energy stored in both the filter inductor and capacitor. But in the flyback, that capacitor is necessarily larger because it is the stored energy in it alone that supplies current to the load during the transistor “on” time. Output ripple is determined mostly by the ESR of the filter capacitor (see Section 1.3.7). An initial selection of the filter capacitor is made on the basis of output ripple specification from Eq. 1.10.

Frequently, however, it is not the output ripple voltage requirement that determines the final choice of the filter capacitor. Ultimately it may be the ripple current rating of the capacitor selected initially on the basis of the output ripple voltage specification.

In a forward-type converter (as in a buck regulator), the capacitor ripple current is greatly limited by the output inductor in series with it (Section 1.3.6). In a flyback, however, the full DC load current flows from common through the capacitor during the transistor “on” time. During the transistor “off” time, a charge of equal ampere-second product must flow into the capacitor to replenish the charge it lost during the “on” time. Assuming, as in Figure 4.1, a sum of “on” time plus reset time of 80% of full period, the RMS ripple current in the capacitor is closely

$$I_{\text{rms}} = I_{\text{dc}} \sqrt{\frac{t_{\text{on}}}{T}} = I_{\text{dc}} \sqrt{0.8} = 0.89 I_{\text{dc}} \quad (4.15)$$

If the capacitor initially selected on the basis of output ripple voltage specifications did not also have the ripple current rating of Eq. 4.15, a larger capacitor or more units in parallel must be chosen.

## 4.7 Universal Input Flybacks for 120-V AC Through 220-V AC Operation

Here we consider universal or wide input range flyback topologies that do not have the auto ranging, voltage doubling methods previously described.

In Section 3.2.1, we considered a commonly used scheme that permitted operation from either a 120-V AC or 220-V AC line with minimal changes. As seen in Figure 3.1 at 120 V AC, switch S1 is thrown to the lower position, making the circuit into a voltage doubler that yields a rectified voltage of 336 V. With 220-V AC, S1 is thrown to the upper position and the circuit becomes a full-wave rectifier with C1 and C2 in series, yielding about 308 V. The converter is thus designed to always work from a rectified nominal input of 308 to 336 V DC by proper choice of the transformer turns ratio.

In some applications, it is preferable to eliminate the requirement of changing S1 from one position to the other in changing from 120- to 220-V AC operation. To change switch position without opening the power supply case, the switch must be accessible externally, and this is a safety hazard. The alternative is to change the switch internally, but this requires opening the power supply case to make the change, and this is a nuisance. Further, there is always the possibility that the switch is mistakenly thrown to the voltage doubling position when operated from 200 V AC. This, of course, would cause significant damage—the power transistor, rectifiers, and filter capacitors would be destroyed.

An alternative is the universal line voltage unit that does not require switching and can tolerate the full range of line inputs from 115 to 220 V AC. The rectified 115 V input will be 160 V DC and the 220 V AC will be 310 V DC.

A flyback converter, designed with a small primary/secondary turns ratio, can ensure that the “off”-voltage stress at high AC input does not overstress the power transistor.

The maximum “on” time  $\overline{T_{on}}$  at the minimum value of the 220-V AC input is calculated from the corresponding minimum rectified DC input as in Eq. 4.7 and the rest of the magnetics design can proceed as shown in the text following Eq. 4.7. The minimum “on” time occurs at the maximum value of the 220-V AC input. Since the feedback loop keeps the product of  $V_{dc}T_{on}$  constant (Eq. 4.3), minimum “on” time is  $\underline{T_{on}} = \overline{T_{on}}(\underline{V_{dc}}/\overline{V_{dc}})$  where  $\underline{V_{dc}}$  and  $\overline{V_{dc}}$  correspond to the minimum and maximum values of the 220-V AC line.

The maximum “on” time with 115-V AC input is still given by Eq. 4.7 and will be greater than with 220 V, as the term  $\underline{V_{dc}} - 1$  is smaller. But the primary inductance  $L_p$  given by Eq. 4.8, which is proportional to the product  $V_{dc}T_{on}$ , is still the same as that product is kept constant by the feedback loop. So long as the transistor can operate with

## 148 Switching Power Supply Design

the minimum “on” time calculated for the maximum DC corresponding to high AC input, there is no problem. With bipolar transistors operating at a high frequency, transistor storage time could prevent operation at too low an “on” time. An example will clarify this.

Eq. 4.4 gives the maximum “off” stress in terms of the maximum DC input voltage, the output voltage, and the  $N_p/N_s$  turns ratio. Assume in that equation that  $\overline{V_{ms}}$  is 500 V; many bipolar transistors can safely sustain that voltage with a negative base bias at turn “off” ( $V_{cev}$  rating). At 220 V AC, the nominal  $V_{dc}$  is 310 V. Assume that the maximum at high line with a worst-case transient is 375 V. Then for a 5-V output, Eq. 4.4 gives a turns ratio of 21.

Now assume that minimum DC supply voltage is 80% of nominal. Assume a switching frequency of 50 kHz (period  $T$  of 20  $\mu$ s). Maximum “on” time is calculated from Eq. 4.7 at the minimum DC input corresponding to minimum AC input of  $0.8 \times 115$  or 92 V AC. For the corresponding DC input of  $1.41 \times 92$  or about 128 V, maximum “on” time calculated from Eq. 4.7 is 7.96  $\mu$ s.

Minimum “on” time occurs at maximum input voltage. Assuming a 20% high line, the maximum DC input is  $1.2 \times 220 \times 1.41 = 372$  V. Since the feedback loop keeps the product of  $V_{dc}T_{on}$  constant (Eq. 4.3), “on” time at the 20% high line of 264 V AC is  $(128/372)(7.96)$  or 2.74  $\mu$ s. The circuit can thus cope with either a 20% low AC line input of 92 V AC from a nominal 115 V AC, or a 20% high AC input of 264 V AC from the nominal 220-V AC line by readjusting its “on” time from 7.96 to 2.74  $\mu$ s.

If this were attempted at higher switching frequencies, the minimum “on” time at a 220-V AC line would become so low as to prohibit the use of bipolar transistors, which could have 0.5- to 1.0- $\mu$ s storage time. The upper-limit switching frequency at which the above scheme can be used with bipolar transistors is about 100 kHz.

It is instructive to complete the above design. Assume an output power of 150 W at 5-V output. Then  $R_o = 0.167 \Omega$  and the primary inductance from Eq. 4.8 is

$$L_p = \left( \frac{0.167}{2.5 \times 20 \times 10^{-6}} \right) \left( \frac{128 \times 7.96 \times 10^{-6}}{5} \right)^2$$

$$= 139 \mu\text{H}$$

and the peak primary current from Eq. 4.9 is

$$I_p = \frac{128 \times 7.96 \times 10^{-6}}{139 \times 10^{-6}} = 7.33 \text{ A}$$

There are many reasonably priced bipolar transistors with a  $V_{cev}$  rating above 500 V having adequate gain at 7.33 A.

Table 4.1 shows that the 55932 MPP core can tolerate a maximum of 480 ampere-turns, beyond which its inductance will fall off by more than 10% (at 5 A, column 9 shows that the maximum turns is 96 for a maximum inductance of 265  $\mu\text{H}$ ). For maximum ampere-turns, the inductance is  $32,000 \times 0.9(66/1000)^2 = 125 \mu\text{H}$ . If (as discussed in Section 4.2.3.2) 10% more turns are added, the inductance at 7.33 A will increase by 10% to 138  $\mu\text{H}$ , but at zero current, the inductance will “swing” up to 20% above that.

If the 20% inductance swing is undesirable, the lower permeability core 55933 of Table 4.1 can be used. Table 4.1 shows that the maximum ampere-turns stress is 859. For 7.33 A, the maximum number of turns is  $859/7.33$  or 117. The maximum inductance for a swing of only 10% is  $(0.117)^2 \times 18000 \times 0.9$  or 222  $\mu\text{H}$ . For the desired 139  $\mu\text{H}$ , the required turns are  $1000 \sqrt{0.139/18 \times 0.95} = 90$ .

Thus a design not requiring voltage doubling/full-wave rectifier switching when operation is changed from 115 to 220 V AC is possible. But this subjects the power transistor to a leakage inductance spike at turn “off” of about 500 V. The lower reliability of this scheme must be weighed against the use of a double-ended forward converter or half bridge—both of which subject the “off” transistor to only the maximum DC input (375 V in the preceding example) with no leakage spike. Of course, for 115/220-V AC operation, the rectifier switching of Figure 3.1 must be accepted.

**After Pressman** *Modern FETs (for example, the Power Integrations “Top Switch” devices) very much simplify the design of universal input flyback type supplies, which are now an accepted and standard topology for lower power applications. Very good application notes are available for these devices. ~K.B.*

## 4.8 Design Relations—Continuous-Mode Flybacks

### 4.8.1 The Relation Between Output Voltage and “On” Time

Look once again at Figure 4.1. When the transistor Q1 is “on,” the voltage across the primary is close to  $V_{dc}-1$  with the dot end negative with respect to the no-dot end, and the core is driven—say, up the hysteresis loop. When the transistor turns “off,” the magnetizing current reverses the polarity of all voltages in order to remain constant. The primary and secondary are driven positive, but the secondary is caught and clamped to  $V_{om} + 1$  by D2—assuming a 1-V forward drop.

## 150 Switching Power Supply Design

This reflects across to the primary as a voltage  $(N_p/N_s)(V_{om} + 1)$ , with the dot end now positive with respect to the no-dot end. All the current that was flowing in the primary ( $I_{pO}$  in Figure 4.2c) now transfers to the secondary as  $I_{TU}$  in Figure 4.2d. The initial magnitude of the secondary current  $I_{TU}$  is equal to the final primary current at the end of the “on” time ( $I_{pO}$ ) times the turns ratio  $N_p/N_s$ . Since the dot end of the secondary is now positive with respect to the no-dot end, the secondary current ramps downward with the slope  $UV$  in Figure 4.2d.

Since the primary is assumed to have zero DC resistance, it cannot sustain a DC voltage averaged over many cycles. Thus in the steady state, the volt-second product across it when the transistor is “on” must equal that across it when the transistor is “off”—i.e., the voltage across the primary averaged over a full cycle must equal zero. This is equivalent to saying the core’s downward excursion on the  $BH$  loop during the “off” time is exactly equal to the upward excursion during the “on” time. Then

$$(\underline{V}_{dc} - 1)\overline{t_{on}} = (V_{om} + 1)\frac{N_p}{N_s}t_{off}$$

or

$$V_{om} = \left[ (\underline{V}_{dc} - 1) \frac{N_s}{N_p} \frac{\overline{t_{on}}}{t_{off}} \right] - 1 \quad (4.16)$$

and since there is no dead time in continuous mode,  $\overline{t_{on}} + t_{off} = T$ , and

$$V_{om} = \left[ \frac{(\underline{V}_{dc} - 1)(N_s/N_p)(\overline{t_{on}}/T)}{1 - \overline{t_{on}}/T} \right] - 1 \quad (4.17a)$$

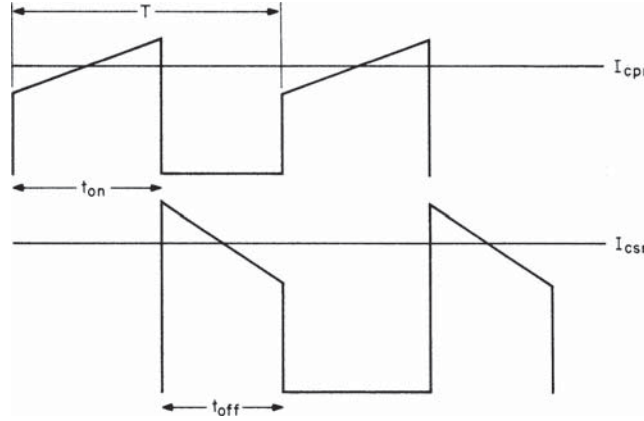
$$= \left[ \frac{(\underline{V}_{dc} - 1)(N_s/N_p)}{(T/\overline{t_{on}}) - 1} \right] - 1 \quad (4.17b)$$

The feedback loop regulates against DC input voltage changes by decreasing  $t_{on}$  as  $V_{dc}$  increases, or increasing  $t_{on}$  as  $V_{dc}$  decreases.

### 4.8.2 Input, Output Current–Power Relations

In Figure 4.6, the output power is equal to the output voltage times the average of the secondary current pulses. For  $I_{csr}$  equal to the current at the center of the ramp in the secondary current pulse

$$\begin{aligned} P_o &= V_o I_{csr} \frac{t_{off}}{T} \\ &= V_o I_{csr} (1 - \overline{t_{on}}/T) \end{aligned} \quad (4.18)$$



**FIGURE 4.6** Real-time relation between the primary and secondary current waveforms in a continuous-mode flyback converter. Current is delivered to the output capacitor only during the “off” period of Q1. At a fixed DC input voltage,  $t_{on}$  and  $t_{off}$  remain constant. Output load current changes are accommodated by the feedback loop by changing the magnitude of the current at the center of the primary current ramp  $I_{cpr}$ , which results in a change at the center of the secondary current ramp ( $I_{csr}$ ). This occurs over many switching cycles by temporary increases in “on” time until the average current pulse amplitudes build up and then relax to the new steady-state values of  $t_{on}$  and  $t_{off}$ .

or

$$I_{csr} = \frac{P_o}{V_o(1 - \overline{t_{on}}/T)} \quad (4.19)$$

In Eqs. 4.18 and 4.19,  $\overline{t_{on}}/T$  is given by Eq. 4.17 for specified values of  $V_{om}$  and  $V_{dc}$ , and turns ratio  $N_s/N_p$  from Eq. 4.4, which was chosen for acceptably low maximum “off”-voltage stress at maximum DC input.

Further, for an assumed efficiency of 80%,  $P_o = 0.8P_{in}$  and  $I_{cpr}$  is equal to the current at the center of the ramp in the primary current pulse:

$$P_{in} = 1.25 \quad P_o = V_{dc} I_{cpr} \frac{\overline{t_{on}}}{T}$$

or

$$I_{cpr} = \frac{1.25 P_o}{(V_{dc})(\overline{t_{on}}/T)} \quad (4.20)$$

## 152 Switching Power Supply Design

**After Pressman** In the continuous mode, the duty cycle is defined by the voltage ratio. Changes in load current try to reflect into the primary, but for transient load changes, the transformer inductance limits the rate of change of current. Hence the first and immediate effect of a transient load increase is to cause a decrease in output voltage, resulting in an increase in the “on” period of Q1 (to increase the primary current). But this results in a further drop in output voltage because there is an immediate decrease in the energy-transferring “off” period (the secondary conducting period). It takes many cycles before the new higher current conditions are established, at which point the duty cycle returns to its original value. This is a dynamic effect intrinsic to the topology and cannot be compensated by the control loop. In terms of control theory, this translates to a right-half-plane-zero. ~K.B.

### 4.8.3 Ramp Amplitudes for Continuous Mode at Minimum DC Input

It has been shown that the threshold of continuous-mode operation occurs when there is just the beginning of a step at the front end of the primary current ramp. Referring to Figure 4.6, the step appears when the current at the center of the primary ramp  $I_{cpr}$  just exceeds half the ramp amplitude  $dI_p$ . That value of  $I_{cpr}$  ( $I_{cpr}$ ) is then the minimum value at which the circuit is still in the continuous mode. From Eq. 4.20,  $I_{cpr}$  is proportional to output power and hence for the minimum output power  $\underline{P}_o$  corresponding to  $\underline{I}_{cpr}$

$$I_{cpr} = \frac{dI_p}{2} = \frac{1.25 \underline{P}_o}{(V_{dc})(\overline{t_{on}}/T)}$$

or

$$dI_p = \frac{2.5 \overline{P}_o}{(V_{dc})(\overline{t_{on}}/T)} \quad (4.21)$$

In Eq. 4.21,  $\overline{t_{on}}$  is taken from Eq. 4.17 at the corresponding value minimum of  $V_{dc}$  ( $\underline{V_{dc}}$ ). The slope of the ramp  $dI_p$  is given by  $dI_p = (\underline{V_{dc}} - 1)\overline{t_{on}}/L_p$ , where  $L_p$  is the primary magnetizing inductance. Then

$$\begin{aligned} L_p &= \frac{(\underline{V_{dc}} - 1)\overline{t_{on}}}{dI_p} \\ &= \frac{(\underline{V_{dc}} - 1)(\underline{V_{dc}})(\overline{t_{on}})^2}{2.5 \overline{P}_o T} \end{aligned} \quad (4.22)$$

Here again,  $\underline{P}_o$  is the minimum specified value of output power and  $\overline{t_{on}}$  is the maximum “on” time calculated from Eq. 4.17 at the minimum specified DC input voltage  $\underline{V_{dc}}$ .

#### 4.8.4 Discontinuous- and Continuous-Mode Flyback Design Example

It is instructive to compare discontinuous- and continuous-mode flyback designs at the same output power levels and input voltages. The magnitudes of the currents and primary inductances will be revealing.

Assume a 50-W, 5-V output flyback converter operating at 50 kHz from a telephone industry prime power source (38 V DC minimum, 60 V maximum). Assume a minimum output power of one-tenth the nominal, or 5 W.

Consider first a discontinuous-mode flyback. Choosing a bipolar transistor with a 150-V  $V_{ce0}$  rating is very conservative, because it is not necessary to rely on the  $V_{cer}$  or  $V_{cev}$  ratings that permit larger voltages. Then in Eq. 4.4, assume that the maximum “off”-voltage stress  $\bar{V}_{ms}$  without a leakage spike is 114 V, which permits a 36-V leakage spike before the  $V_{ce0}$  limit is reached. Then Eq. 4.4 gives  $N_p/N_s = (114 - 60)/6 = 9$ .

Eq. 4.7 gives the maximum “on” time as

$$\begin{aligned}\bar{t}_{on} &= 6 \times 9 \times 0.8 \frac{20 \times 10^{-6}}{37 + 6 \times 9} \\ &= 9.49 \mu\text{s}\end{aligned}$$

and primary inductance for  $R_o = 5/10 = 0.5 \Omega$  from Eq. 4.8 is

$$\begin{aligned}L_p &= \frac{0.5}{2.5 \times 10^{-6}} \left( \frac{38 \times 9.49}{5} \right)^2 \times 10^{-12} \\ &= 52 \mu\text{H}\end{aligned}$$

Peak primary current from Eq. 4.9 is

$$\begin{aligned}I_p &= \frac{38 \times 9.49 \times 10^{-6}}{52 \times 10^{-6}} \\ &= 6.9 \text{ A}\end{aligned}$$

and the start of the secondary current triangle is

$$I_{s(\text{peak})} = (N_p/N_s)I_p = 9 \times 6.9 = 62 \text{ A}$$

Recall that in the discontinuous flyback, the reset time  $Tr$ —the time for the secondary current to decay back to zero—plus the maximum “on” time is equal to  $0.8T$  (Eq. 4.6). Reset time is then  $T_r = (0.8 \times 20) - 9.49 = 6.5 \mu\text{s}$ , and the average value of the secondary current triangle (which



## 154 Switching Power Supply Design

should equal the DC output current) is

$$\begin{aligned} I \text{ (secondary average)} &= \frac{I_{s(\text{peak})}}{2} \frac{T_r}{T} \\ &= \left( \frac{62}{2} \right) \frac{6.5}{20} = 10 \text{ A} \end{aligned}$$

which is the DC output current.

Now consider a continuous-mode flyback for the same frequency, input voltages, output power, output voltage, and the same  $N_p/N_s$  ratio of 9. From Eq. 4.17b, calculate  $\overline{f_{\text{on}}}/T$  for  $V_{\text{dc}} = 38 \text{ V}$  as

$$5 = \left[ \frac{(37/9)(\overline{f_{\text{on}}}/T)}{1 - \overline{f_{\text{on}}}/T} \right] - 1$$

or  $\overline{f_{\text{on}}}/T = 0.5934$  and  $\overline{f_{\text{on}}} = 11.87 \mu\text{s}$ ,  $t_{\text{off}} = 8.13 \mu\text{s}$  and from Eq. 4.19

$$I_{\text{csr}} = \frac{50}{(5)(1 - 0.5934)} = 24.59 \text{ A}$$

and the average of the secondary current pulse, which should equal the DC output current, is

$$I \text{ (secondary average)} = I_{\text{csr}}(t_{\text{off}}/T) = 24.59 \times 8.13/20 = 10.0 \text{ A}$$

which checks. From Eq. 4.20,  $I_{\text{cpr}} = 1.25 \times 50/(38)(11.86/20) = 2.77 \text{ A}$ .

From Eq. 4.22, for the minimum input power of 5 W at the minimum DC input voltage of 38 V,  $L_p = 37 \times 38(11.86)^2 \times 10^{-12}/2.5 \times 5 \times 20 \times 10^{-6} = 791 \mu\text{H}$ .

The contrast between the discontinuous and continuous modes will now be clear from the following table, which compares the required primary inductances, and primary and secondary currents at minimum DC input of 38 V.

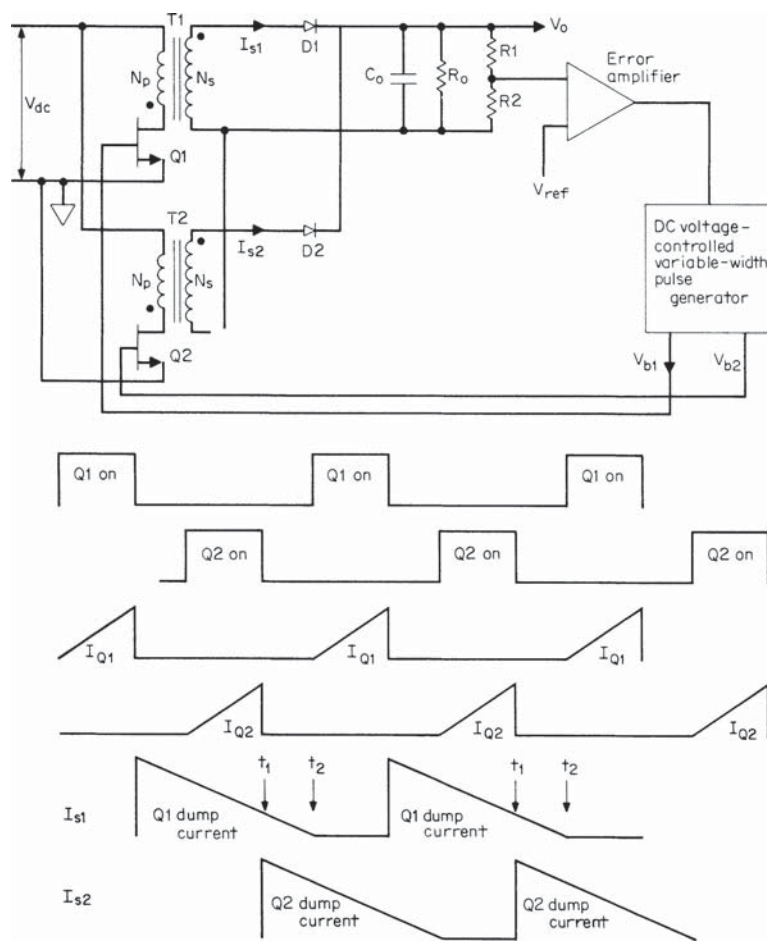
	Discontinuous	Continuous
Primary inductance, $\mu\text{H}$	52	791
Primary peak current, A	6.9	2.77
Secondary peak current, A	62.0	24.6
On time, $\mu\text{s}$	9.49	11.86
Off time, $\mu\text{s}$	6.5	8.13

The lower primary current and especially the secondary current for the continuous mode are certainly an advantage, but the much larger primary inductance that slows up response to load current changes, and the right-half-plane-zero that requires a very low error-amplifier

bandwidth to achieve loop stabilization, can make the continuous mode a less desirable choice in applications that require good transient load response. In fixed-load applications this is not a problem.

## 4.9 Interleaved Flybacks

An interleaved flyback topology is shown in Figure 4.7. It consists of two or more discontinuous-mode flybacks whose power transistors



**FIGURE 4.7** Interleaving two discontinuous-mode flybacks on alternative half cycles to reduce peak currents. Output powers of up to 300 W are possible with reasonably low peak currents.

## 156 Switching Power Supply Design

are turned “on” at alternate half cycles and whose secondary currents are summed through their rectifying diodes.

It can be used at power levels up to 300 W, limited mainly by the high-peak primary and especially secondary currents. Although that power level can be obtained with a single continuous-mode flyback with reasonable currents, it may be better to accept the greater cost and volume of two or more interleaved discontinuous-mode flybacks. Both input and output ripple currents are much smaller and of higher frequency. Increasing the number of elements with suitable phase shift between drive pulses will further reduce the ripple current. Further, the discontinuous mode’s faster response to load current changes, greater error-amplifier bandwidth, and the elimination of the right-half-plane-zero loop stabilization problem may make this a preferred choice.

A single discontinuous-mode flyback at the 300-W level is impractical because of the very high peak primary and secondary currents, as can be seen from Eqs. 4.2, 4.7, and 4.8.

At a lower power of 150 W, a single forward converter is very likely a better choice than the two interleaved flybacks because of the considerably lower secondary peak current of the forward converter. The interleaved flyback has been shown here for the sake of completeness and for its possible use at lower power levels when many (over five) outputs are required.

### 4.9.1 Summation of Secondary Currents in Interleaved Flybacks

The magnetics design of each flyback in an interleaved flyback proceeds exactly as for a single flyback at half the power level, because the secondary currents add into the output through their “ORing” rectifier diodes.

Even when both secondary diodes dump current simultaneously (as from  $t_1$  to  $t_2$ ), there is no possibility that one diode can back-bias the other and supply all the load current. This can happen if one attempts to sum the currents of two low-impedance voltage sources. If one of the low-impedance voltage sources has a slightly higher open-circuit voltage or a lower forward-drop or diode, it will back-bias the other diode and supply all the load current by itself. This can over-dissipate the diode or the transistor supplying that diode.

Looking back into the secondary of a flyback, however, there is a high-impedance current source, which is the secondary inductance. Thus the current dumped into the common load by either diode is unaffected by the other diode simultaneously supplying load current.

## 4.10 Double-Ended (Two Transistor) Discontinuous-Mode Flyback

### 4.10.1 Area of Application

The topology is shown in Figure 4.8a. Its major advantage is that, using the scheme of the double-ended forward converter of Figure 2.13, its power transistors in the “off” state are subjected to only the maximum DC input voltage. This is a significant advantage over the single-ended forward converter of Figure 4.1, where the maximum “off”-voltage stress is the maximum DC input voltage plus the reflected secondary voltage  $(N_p/N_s)(V_o + 1)$  plus a leakage inductance spike that may be as high as one-third of the DC input voltage.

### 4.10.2 Basic Operation

The lower “off”-voltage stress comes about in the same way as for the double-ended forward converter of Figure 2.13. Power transistors  $Q_1$ ,  $Q_2$  are turned “on” simultaneously. When they are “on,” the dot end of the secondary is negative,  $D_3$  is reverse-biased, and no secondary current flows. The primary is then just an inductor, and current in it ramps up linearly at a rate of  $dI_1/dt = V_{dc}/(L_m + L_l)$ , where  $L_m$  and  $L_l$  are the primary magnetizing and leakage inductances, respectively. When  $Q_1$  and  $Q_2$  turn “off,” as in the previous flybacks, all primary and secondary voltages reverse polarity,  $D_3$  becomes forward-biased, and the stored energy in  $L_m = 1/2 L_m (I_1)^2$  is delivered to the load.

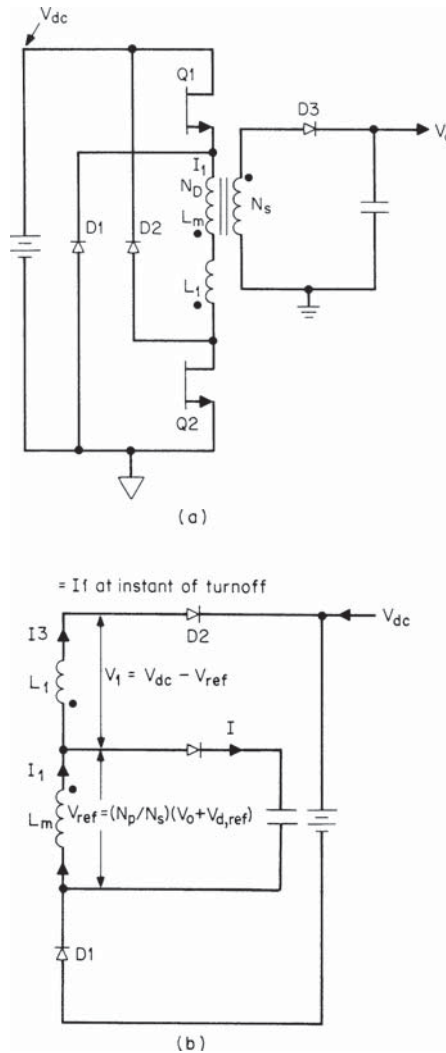
As shown previously, the “on” or set volt-second product across the primary must equal the “off” or reset volt-second product. At the instant of turn “off,” the bottom end of  $L_l$  attempts to go far positive but is clamped to the positive end of  $V_{dc}$ . The top end of  $L_m$  attempts to go far negative but is clamped to the negative end of  $V_{dc}$ . Thus the maximum voltage stress at either  $Q_1$  or  $Q_2$  can never be more than  $V_{dc}$ .

The actual resetting voltage  $V_r$  across the magnetizing inductance  $L_m$  during the “off” time is given by the voltage reflected from the secondary  $(N_p/N_s)(V_o + V_{D3})$ . The voltage across  $L_m$  and  $L_l$  in series is the DC supply voltage, and hence, as seen in Figure 4.8b, the voltage across the leakage inductance  $L_l$  is  $V_l = (V_{dc} - V_r)$ .

The division of the  $V_{dc}$  supply voltage across  $L_m$  and  $L_l$  in series during the “off” time is a very important point in the circuit design and establishes the transformer turns ratio  $N_p/N_s$  as discussed below.

The price paid for this advantage is, of course, the requirement for two transistors and the two clamp diodes,  $D_1$ ,  $D_2$ .

## 158 Switching Power Supply Design



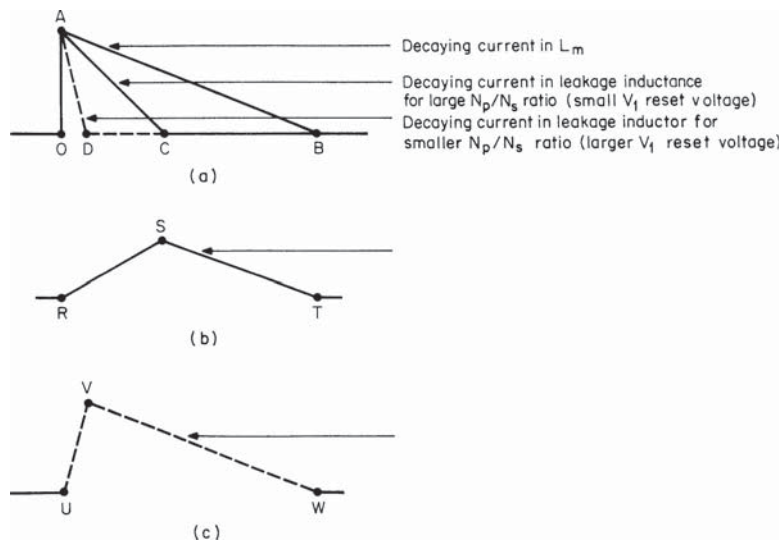
**FIGURE 4.8** Circuit during Q1 and Q2 “off” time. Current  $I_1$ , stored in  $L_m$  during Q1, Q2 “on” time, also flows through leakage inductance  $L_l$ . During the “off” time, energy stored in  $L_m$  must be delivered to the secondary load as reflected into the primary across  $L_m$ . But  $I_1$  also flows through  $L_l$ , and during the “off” time, the energy it represents ( $\frac{1}{2}L_l I^2$ ) is returned to the input source  $V_{dc}$  through diodes D1, D2. This robs energy that should have been delivered to the output load and continues to rob energy until  $I_1$ , the leakage inductance current, falls to zero. To minimize the time for  $I_1$  in  $L_l$  to fall to zero,  $V_i$  is made significantly large by keeping the reflected voltage  $V_r (= N_p/N_s)(V_o + V_{d3,ref})$  low by setting a low  $N_p/N_s$  turns ratio. A usual value for  $V_r$  is two-thirds of the minimum  $V_{dc}$ , leaving one-third for  $V_i$ .

### 4.10.3 Leakage Inductance Effect in Double-Ended Flyback

Figure 4.8b shows the circuit during the Q1, Q2 “off” time. The voltage across  $L_m$  and  $L_l$  in series is clamped to  $V_{dc}$  through diodes D1, D2. The voltage  $V_r$  across the magnetizing inductance is clamped against the reflected secondary voltage and equals  $(N_p/N_s)(V_o + V_{D3})$ . The voltage across  $L_l$  is then  $V_l = V_{dc} - V_r$ .

At the instant of turn “off,” the same current  $I_1$  flows in  $L_m$  and  $L_l$  ( $I_3 = I_1$  at instant of turn “off”). That current in  $L_l$  flows through diodes D1, D2 and returns its stored energy to the supply source  $V_{dc}$ . The  $L_l$  current decays at a rate of  $dI_1/dt = V_l/L_l$  as shown in Figure 4.9a as slope AC or AD. The current in  $L_m$  (initially also equal to  $I_1$ ) decays at a rate  $V_r/L_m$  and is shown in Figure 4.9a as slope AB.

The current actually delivering power to the load is  $I_2$ —the difference between the currents in  $L_m$  and  $L_l$ . This is shown as current RST in Figure 4.9b if the  $L_l$  current slope is AC of Figure 4.9a. The larger area current UVW in Figure 4.9c results if the  $L_l$  current slope is faster, as AD of Figure 4.9a. It should be evident in Figures 4.9b and 4.9c that so long as current still flows in leakage inductance  $L_l$ , through D1 and D2 back into the supply source, all the current available in  $L_m$  does



**FIGURE 4.9** (a) Currents in magnetizing and leakage inductances in double-ended flyback. (b) Current into reflected load impedance for large  $N_p/N_s$  ratio. AB–AC of Figure 4.9a. (c) Current into reflected load impedance for smaller  $N_p/N_s$  ratio. AB–AD of Figure 4.9a.

## 160 Switching Power Supply Design

not flow into the reflected load but is partly diverted back into the supply.

It can thus be seen from Figures 4.9*b* and 4.9*c* that to maximize the transfer of  $L_m$  current to the reflected load and to avoid a delay in the transfer of current to the load, the slope of the leakage inductance current decay should be maximized (slope  $AD$  rather than  $AC$  in Figure 4.9*a*). Or in magnetics–power supply jargon, the leakage inductance current should be rapidly reset to zero.

Since the rate of decay of the leakage inductance current is  $V_l/L_l$  and  $V_l = V_{dc} - (N_p/N_s)(V_o + V_{D3})$ , choosing lower values of  $N_p/N_s$  increases  $V_l$  and hastens leakage current reset. A usual value for the reflected voltage  $(N_p/N_s)(V_o + V_{D3})$  is two-thirds of  $V_{dc}$ , leaving one-third for  $V_l$ . Too low a value for  $V_l$  will require a longer time to reset the magnetizing inductance, rob from the available  $Q1$ ,  $Q2$  “on” time, and decrease the available output power.

Once  $N_p/N_s$  has been fixed to yield  $V_l = V_{dc}/3$ , the maximum “on” time for discontinuous operation is calculated from Eq. 4.7,  $L_m$  is calculated from Eq. 4.8 and  $I_p$  from Eq. 4.9, just as for the single-ended flyback.

---

## References

1. Billings, K., *Switchmode Power Supply Handbook*, McGraw-Hill, New York, 1989.
2. Chryssis, G., *High Frequency Switching Power Supplies*, 2nd Ed., McGraw-Hill, New York, 1989, pp. 122–131.
3. Dixon, L., “The Effects of Leakage Inductance on Multi-output Flyback Circuits,” *Unitrode Power Supply Design Seminar Handbook*, Unitrode Corp., Lexington, Mass., 1988.
4. Patel, R., D. Reilly, and R. Adair, “150 Watt Flyback Regulator,” *Unitrode Power Supply Design Seminar Handbook*, Unitrode Corp., Lexington, Mass., 1988.

# CHAPTER 5

## Current-Mode and Current-Fed Topologies

### 5.1 Introduction

In this chapter, current-mode<sup>1–7</sup> and current-fed<sup>9–20</sup> topologies are grouped into one family, despite their very significant differences, because they both rely on controlling input current and output voltage. However, they do this in quite different ways.

#### 5.1.1 Current-Mode Control

Current-mode control (Figure 5.3) has two control loops: a slow outer loop (via  $R1, R2$  and error amp EA), which senses DC output voltage and delivers a control voltage ( $V_{eao}$ ), to a much faster inner current control loop (via  $R1, V_i$ , and the pulse width modulator PWM).  $R_i$  senses peak transistor currents (the peak choke current) and keeps the peak current constant on a pulse-by-pulse basis. The end result is that it solves the magnetic flux imbalance problem in the current-mode version of the push-pull topology and restores push-pull as a viable approach in applications where the uncertainty of other solutions to flux imbalance is a drawback (Section 2.2.8). Further, the constant power transistor current pulses simplify the feedback-loop design.

**After Pressman** *Because the converter in this example is a forward type, the secondary current reflects back into the primary. By sensing the current in the common return of Q1 and Q2, the inner current control loop effectively is looking at the current flow in the output choke  $L_o$ . The fast inner loop maintains the peak current in  $L_o$  constant on a pulse-by-pulse basis, changing only slowly in response to voltage adjustments. In this way, the peak output current in  $L_o$  is the controlled parameter. This takes  $L_o$  out of the small signal transfer function of the outer loop, allowing faster response in the closed loop system. At the same time, because current is the controlled parameter, current*



## 162 Switching Power Supply Design

*limit and short circuit protection are intrinsic in the topology. Further, since current is controlled on a pulse-by-pulse basis, any tendency for current imbalance in Q1 and Q2 is eliminated and staircase saturation of T1 is no longer a possibility. Finally, the effect of any changes in supply voltage is automatically eliminated from the peak output current in  $L_o$ , so that line regulation is automatically better. ~K.B.*

### 5.1.2 Current-Fed Topology

A current-fed topology derives its input current from an input inductor (choke) as shown in Figure 5.9. In this example, the top end of a push-pull forward converter transformer gets its supply from input inductor  $L_1$ . Thus the power train is driven from the high impedance current source (the input inductor  $L_1$ ) rather than the low impedance of a rectifier filter capacitor or perhaps the low-source impedance of a source battery. This higher source impedance helps to solve the flux imbalance problem in T1 and offers other significant advantages.

---

## 5.2 Current-Mode Control

In all the voltage-mode topologies discussed so far, output voltage alone is the controlled parameter. In those circuits, regulation against load current changes occurs because current changes cause small output voltage changes that are sensed by a voltage-monitoring error amplifier, which then corrects the power transistor “on” time to maintain output voltage constant. Output current itself is not monitored directly.

In the 1980s, the new topology *current-mode control* appeared, in which both voltage and current were monitored. The scheme had been known previously, but was not widely used as it required discrete circuit components to implement it. When a new Unitrode™ pulse-width-modulating (PWM) chip—the UC1846—appeared, with all the features needed to implement current-mode control, the advantages of the technique were quickly recognized and it was widely adopted.

**After Pressman** *As of 2008, many similar current-mode control ICs are now available. Unitrode is now part of Texas Instruments. ~K.B.*

Where two 180° out-of-phase width-modulated drive signals are required as in the push-pull, half-bridge, full-bridge, interleaved forward converter, or flyback, the UC1846 can be used to implement current-mode control. A lower-cost, single-ended PWM controller, the UC1842, is currently available to implement current mode in

single-ended circuits such as forward converters, flybacks, and buck regulators.

## 5.2.1 Current-Mode Control Advantages

### 5.2.1.1 Avoidance of Flux Imbalance in Push-Pull Converters

Flux imbalance was discussed in Section 2.2.5. It occurs in a push-pull converter when the transformer core operates asymmetrically about the origin of its hysteresis loop. The consequence is that the core moves up toward saturation and one transistor draws more current during its “on” time than does the opposite transistor (Figure 2.4c).

As the core drifts further off center of the origin, it goes deeply into saturation and may destroy the power transistor. A number of ways to cope with flux imbalance have been described in Section 2.2.8. These schemes work, but under unusual line or load transient conditions and especially at higher output powers, there is never complete certainty that flux imbalance cannot occur.

Current-mode monitors current on a pulse-by-pulse basis and forces alternate pulses to have equal peak amplitudes by correcting each transistor’s “on” time so that current amplitudes must be equal. This puts push-pull back into the running in any proposed new design and is a valuable contribution to the repertoire of possible topologies. For example, if a forward converter with no flux imbalance problem were chosen to be certain of no flux imbalance in the absence of current mode, a severe penalty would be paid.

Eq. 2.28 shows the peak primary current in a forward converter is  $3.13(P_o/V_{dc})$ . But Eq. 2.9 shows it is only half that or  $1.56(P_o/V_{dc})$  for the push-pull. At low output powers, it is not a serious drawback to use the forward converter with twice the peak current of a push-pull at equal output power, especially since the forward converter has only one transistor. But at higher output power, twice the peak primary current in a forward converter than in a push-pull becomes prohibitive.

The push-pull is a very attractive choice for telephone industry power supplies where the maximum DC input voltage is specified as only 38–60 V. Having it in its current-mode version with a certainty that flux imbalance cannot exist is very valuable.

### 5.2.1.2 Fast Correction Against Line Voltage Changes

#### Without Error Amplifier Delay (Voltage Feed-Forward)

It is inherent in the details of how current mode works that a line voltage change immediately causes a change in power transistor “on” time. This change is corrected without having to wait for an output voltage change to be sensed after a relatively long delay by a

## 164 Switching Power Supply Design

conventional voltage error amplifier. The details of how this comes about will be discussed below.

### 5.2.1.3 Ease and Simplicity of Feedback-Loop Stabilization

All the topologies discussed above with the exception of flybacks have an output  $LC$  filter. An  $LC$  filter has a maximum possible phase shift of  $180^\circ$  not far above its resonant frequency of  $f_o = \frac{1}{2\pi\sqrt{LC}}$ , and gain between input and output falls very rapidly with increasing frequency. As frequency increases, the impedance of the series  $L$  arm increases and that of the shunt arm decreases.

This possible large phase shift and rapid change of gain with frequency complicates feedback-loop design. More important, the elements around the error amplifier required to stabilize the loop are more complex and can cause problems with rapid changes in input voltage or output current.

In a small-signal analysis of the current-mode outer voltage loop, however, which calculates gain and phase shift to consider the possibility of oscillation, the output inductor does not appear even though it is physically in series with the output shunt capacitor. So for small signal changes, the voltage loop behaves as if the inductor were not there.

The circuit behaves as if there were a constant current feeding the parallel combination of the output capacitor and the output load resistor. Such a network can yield only  $90^\circ$  rather than  $180^\circ$  of phase shift, and the gain between input and output falls half as rapidly as for a true  $LC$  filter ( $-20$  dB per decade rather than  $-40$  dB per decade). This simplifies feedback-loop design, simplifies the circuitry around the error amplifier required for stabilization, and avoids problems arising from rapid line or load changes. The details of why this is so will be discussed below.

### 5.2.1.4 Paralleling Outputs

A number of current-mode power supplies may be operated in parallel, each with an equal share of the total load current. This is achieved by sensing current in each supply with equal current sensing resistors, which convert transistor peak current pulses to voltage pulses. These are compared in a voltage comparator to a common error-amplifier output voltage, which forces peak current-sensing voltages and hence peak currents in the parallel supplies to be equal.

### 5.2.1.5 Improved Load Current Regulation

Current mode has better load current regulation than voltage mode. The improvement is not as great as that in voltage regulation, however, which is greatly enhanced by the feed-forward characteristic inherent

in current mode. The improved load current regulation comes about because of the greater error-amplifier bandwidth possible in current mode.

### 5.3 Current-Mode vs. Voltage-Mode Control Circuits

To understand the differences and advantages of current mode over voltage mode, it is essential first to see how voltage-mode control circuitry works. The basic elements of a typical voltage-mode, PWM control circuit are shown in Figure 5.1. That block diagram shows most of the elements of the SG1524, the first of many integrated-circuit control chips that have revolutionized the switching power supply industry. The SG1524, originally made by Silicon General Corporation, is now manufactured by many other companies and in improved versions such as the UC1524A (Unitrode) and SG1524B (Silicon General).

#### 5.3.1 Voltage-Mode Control Circuitry

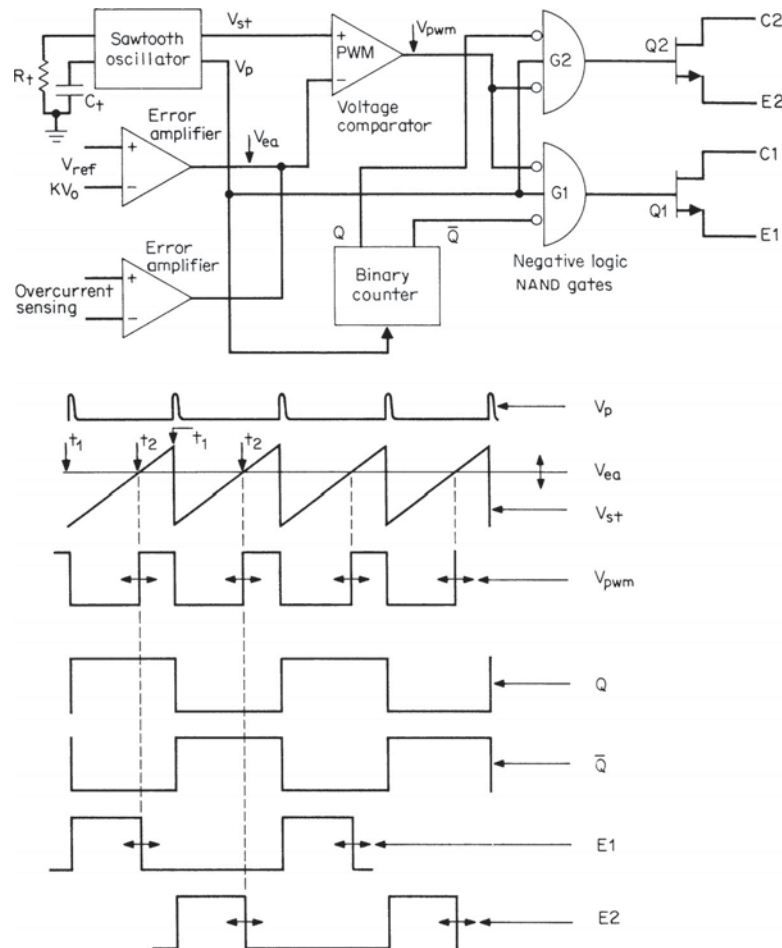
In Figure 5.1, an oscillator generates a 3-V sawtooth  $V_{st}$ . The DC voltage at the triangle base is about 0.5 V and, at the peak, about 3.5 V. The period of the sawtooth is set by external discrete components  $R_t$  and  $C_t$  and is approximately equal to  $T = R_t C_t$ .

An error amplifier compares a fraction of the output voltage  $KV_o$  to a voltage reference  $V_{ref}$  and produces an error voltage  $V_{ea}$ .  $V_{ea}$  is compared to the sawtooth  $V_{st}$  in a voltage comparator (PWM). Note that the fraction of the output  $KV_o$  is fed to the inverting input of the error amplifier so that when  $V_o$  goes up, the error-amplifier output  $V_{ea}$  goes down.

In the PWM voltage comparator, the sawtooth is fed to the non-inverting input and  $V_{ea}$  is fed to the inverting input. Thus the PWM output is a negative-going pulse of variable width. The pulse is negative for the entire time the sawtooth is below the DC level of the error-amplifier output  $V_{ea}$  or from  $t_1$  to  $t_2$ . As the DC output voltage goes—say—slightly positive,  $KV_o$  goes slightly positive, and  $V_{ea}$  goes negative and closer to the bottom of the sawtooth. Thus the duration of the negative-going pulse  $V_{pwm}$  decreases.

The duration of this negative-going pulse is the duration of the power transistor “on” time. Further, since in all the voltage-mode topologies discussed above, the DC output voltage is proportional to the power transistor “on” time, decreasing the “on” time brings the DC output voltage back down by negative-feedback loop action. The duration of the negative pulse  $V_{pwm}$  increases as the output DC voltage decreases.

## 166 Switching Power Supply Design



**FIGURE 5.1** A basic voltage-mode PWM controller. The output voltage is sensed directly by the error amplifier. Regulation against load current changes occurs only after the current changes cause small output voltage changes. The current-limit amplifier operates to shut down the supply only when a maximum current limit is exceeded. Transistor "on" time is from start of sawtooth until the sawtooth crosses  $V_{ea}$ .

The UC1524 is designed primarily for push-pull-type topologies, so the single negative-going pulse of adjustable width, coming once per sawtooth period, must be converted to two  $180^\circ$  out-of-phase pulses of the same width. This is done with the binary counter and negative logic NAND gates  $G_1$  and  $G_2$ . A positive-going pulse  $V_p$  occurring at the end of each sawtooth is taken from the sawtooth oscillator and used to trigger the binary counter.

Outputs from the binary counter  $Q$  and  $\bar{Q}$  are then out-of-phase square waves at half the sawtooth frequency. When they are negative, these square waves steer negative  $V_{\text{pwm}}$  pulses alternately through negative logic NAND  $G_1$  and  $G_2$ . These gates produce a positive output only for the duration of time that the inputs are negative. Thus the bases (and emitters) of output transistors  $Q_1$  and  $Q_2$  are positive only on alternate half cycles and only for the same duration as the  $V_{\text{pwm}}$  negative pulses.

The “on” time of the power transistors must correspond to the time the  $V_{\text{pwm}}$  pulse is negative for the complete circuit to have negative feedback, since  $KV_o$  is connected to the inverting terminal of the error amplifier. Thus if the power transistors are of the NPN type, they must be fed from the emitters of  $Q_1$ ,  $Q_2$ , or if of the PNP type, from the collectors. If current amplifiers are interposed between the bases of the output transistors and  $Q_1$ ,  $Q_2$ , polarities must be such that  $Q_1$ ,  $Q_2$  are “on” when the output transistors are “on.”

The narrow positive pulse  $V_p$  is fed directly into gates  $G_1$ ,  $G_2$ . This forces both gate outputs to be “low” simultaneously for the duration of  $V_p$ , and both output transistors to be “off” for that duration. This ensures that if the pulse width of  $V_{\text{pwm}}$  ever approached a full half period, both power transistors could never be “on” simultaneously at the end of the half period. In a push-pull topology, if both transistors are simultaneously “on” even for a short time, they are subjected to both high current and the full supply voltage and could be destroyed.

This, then, is a voltage-mode circuit. Power transistor or output current is not sensed directly. The power transistors are turned “on” at the beginning of a half period and turned “off” when the sawtooth  $V_{\text{st}}$  crosses the DC level of the error-amplifier output, which is a measure of output voltage only.

The complete details of the SG1524 are shown in Figure 5.2a. The negative logic NAND gates  $G_1$ ,  $G_2$  of Figure 5.1 are shown in Figure 5.2a as positive logic NOR gates. These perform the same function for requiring all “lows” to make a “high” and are identical to any one “high” forcing a “low.”

In Figure 5.2a, when pin 10 goes “high,” the associated transistor collector goes “low” and brings the error-amplifier output (pin 9) down to the base of the sawtooth. This reduces output transistor “on” times to zero and shuts down the supply. In the current limit comparator, if pin 4 is 200 mV more positive than pin 5, the error-amplifier output is also brought down to ground (there is an internal phase inversion, not shown) and the supply is shut down. Pins 4 and 5 are bridged across a current-sensing resistor in series with the current being monitored. If current is to be limited to  $I_m$ , the resistor is selected as  $R_s = 0.2/I_m$ .

## 168 Switching Power Supply Design

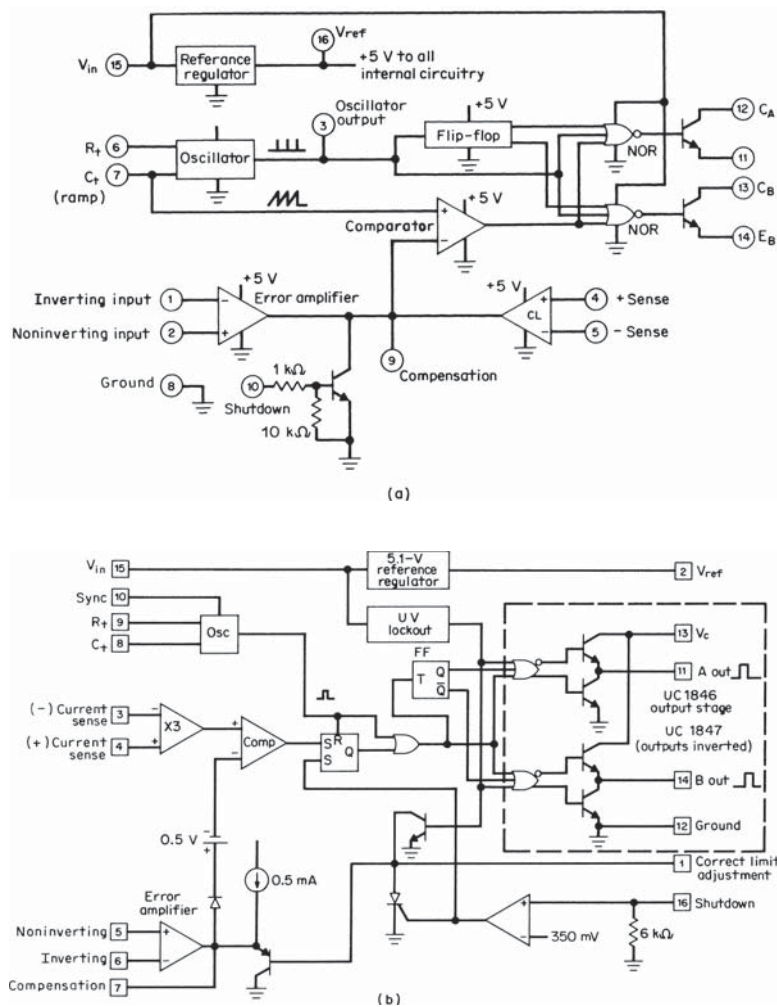


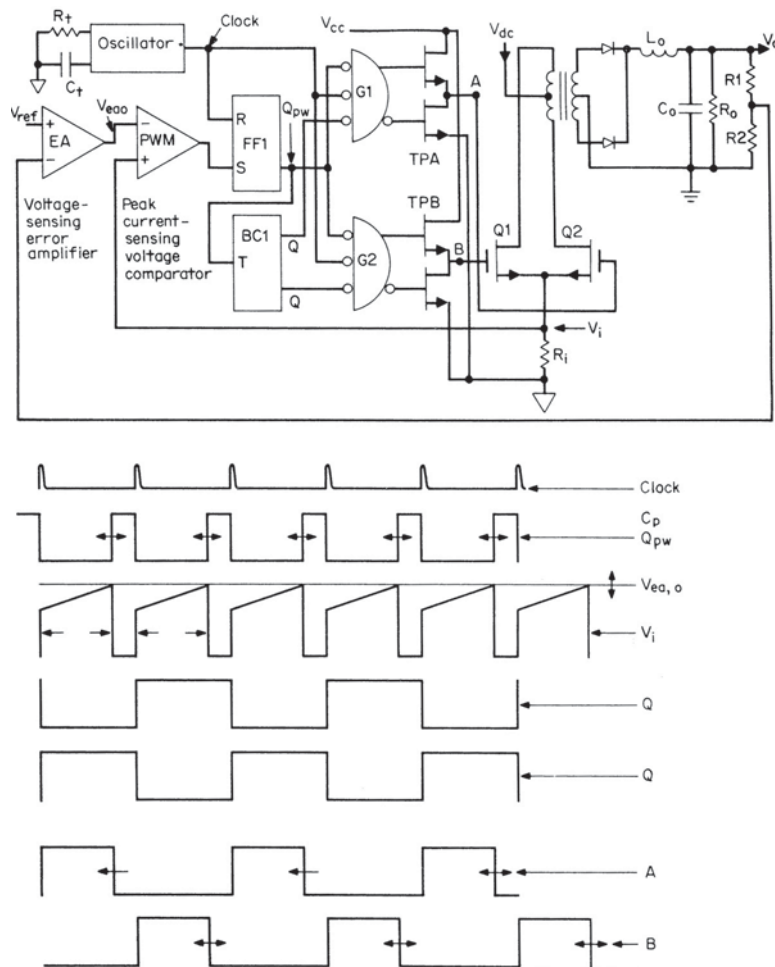
FIGURE 5.2 (a) PWM chip SG1524, the first integrated-circuit pulse-width-modulating control chip. (Courtesy Silicon General Corp.)  
 (b) PWM chip UC1846, Unitrode's first integrated-circuit current-mode control chip. (Courtesy Unitrode Corp.)



### 5.3.2 Current-Mode Control Circuitry

Circuitry of the first integrated-circuit current-mode control chip (Unitrode UC1846) is shown in Figure 5.2*b*. Figure 5.3 shows its basic elements controlling a push-pull converter.

Note in Figure 5.3 that there are two feedback loops—an outer loop consisting of output voltage sensor (EA) and an inner loop comprising



**FIGURE 5.3** Current-mode controller UC1846, driving a push-pull MOSFET converter. Transistors are turned “on” alternately at each clock pulse. They are turned “off” when the peak voltage across the common current-sensing resistor equals the output voltage of the voltage-sensing error amplifier. PWM forces all  $Q_1$ ,  $Q_2$  current pulses to have equal peak amplitudes.



## 170 Switching Power Supply Design

primary peak current sensor (PWM) and current-sensing resistor  $R_i$  which converts ramp-on-a-step transistor currents to ramp-on-a-step voltages.

Line and load current changes are regulated by varying power transistor "on" time. "On" time is determined by both the voltage-sensing error-amplifier output  $V_{eao}$  and the PWM voltage comparator, which compares  $V_{eao}$  to the ramp-on-a-step voltage at the top of the current-sensing resistor  $R_i$ .

Because the secondaries all have output inductors, the secondary currents have the characteristic ramp-on-a-step shape. These reflect as identical-shaped currents, which are smaller by the  $N_s/N_p$  ratio, in the primary and the output transistors. Those currents flowing in the common emitters through  $R_i$  produce the ramp-on-a-step voltage waveshape  $V_i$ . Power transistor "on" time is then determined as follows: An internal oscillator, whose period is set by external discrete components  $R_t$ ,  $C_t$ , generates narrow clock pulses  $C_p$ . The oscillator period is approximately  $0.9R_tC_t$ . At every clock pulse, feed-forward FF1 is reset, causing its output  $Q_{pw}$  to go "low." The duration of the "low" time at  $Q_{pw}$ , it will soon be seen, is the duration of the "high" time at either of the chip outputs  $A$  or  $B$  and, hence, the duration of the power transistor "on" times.

When the PWM voltage comparator output goes "high," FF1 is set, thus terminating the  $Q_{pw}$  "low" and hence the "high" time at  $A$  or  $B$ , and turns "off" the power transistor which had been "on." Thus the instant at which the PWM comparator output goes "high" determines the end of the "on" time.

The PWM comparator compares the ramp-on-a-step current-sensing voltage  $V_i$  to the output of the voltage error-amplifier EA. Hence when the peak of  $V_i$  equals  $V_{eao}$ , the PWM output goes positive and sets FF1,  $Q_{pw}$  goes "high," and whichever of  $A$  or  $B$  had been "high" goes "low." The power transistor that had just been "on" is now turned "off."

A "low" output from FF1 occurs once per clock period. It starts "low" at every clock pulse and goes back "high" when the PWM non-inverting input equals the DC level of the EA output. Most frequently, power transistors  $Q_1$ ,  $Q_2$  will be N types, which require positive-going signals for turn "on." Thus these equal-duration negative-going pulses are steered alternately through negative logic NAND gates  $G_1$  and  $G_2$ , becoming 180° out-of-phase, positive-going pulses at the chip outputs  $A$  and  $B$ .

Chip output stages  $TPA$  and  $TPB$  are "totem poles." When the bottom transistor of a totem pole is "on," the top one is "off" and vice versa. Output nodes  $A$  and  $B$  have very low output impedance. When the bottom transistor is "on," it can "sink" (absorb inward-directed current) 100 mA continuous and 400 mA during the "high"-to-"low" transition. When the top transistor is "on," it can "source"

(emit outward-directed current) 100 mA continuous and 400 mA during the “low”-to-“high” transition.

Steering is done by binary counter  $BC1$ , which is triggered once per clock pulse on the leading edge of the pulse. The negative-going  $Q$  pulses steer the negative  $Q_{pw}$  pulses alternately through negative logic NAND gates  $G1$ ,  $G2$ . The chip outputs  $A$  and  $B$  are  $180^\circ$  out-of-phase positive pulses whose duration is the same as that of the negative pulses  $Q_{pw}$ .

Note that  $Q_{pw}$  is positive from the end of the “on” time until the start of the next turn “on.” This forces the bubble outputs of  $G1$ ,  $G2$  “high” and brings points  $A$  and  $B$  both “low.” This “low” at both power transistor inputs during the dead time between the turn “off” of one transistor and the turn “on” of the other is a valuable feature. It presents a low impedance at the “off”-voltage level and prevents noise pickup from turning the power transistors “on” spuriously. While the bubble outputs of  $G1$ ,  $G2$  are both “high,” their no-bubble outputs are both “low,” and thus turn “off” the upper transistors of the totem poles  $TPA$  and  $TPB$  and avoid over-dissipating them.

It can be seen also that the narrow positive clock pulse is fed as a third input to NAND gates  $G1$ ,  $G2$ . This makes bubble outputs from  $G1$ ,  $G2$  “high” and outputs  $A$ ,  $B$  simultaneously “low” for the duration of the clock pulse. This guarantees that under fault conditions, if the controller attempts a full half period “on” time ( $Q_{pw}$  “low” and either  $A$  or  $B$  “high” for a full half period), there will be a dead time between the end of one “on” time and the start of the opposite “on” time. Thus the power transistors can’t conduct simultaneously.

## 5.4 Detailed Explanation of Current-Mode Advantages

### 5.4.1 Line Voltage Regulation

Consider how the controller regulates against line voltage changes. Assume that line voltage (and hence  $V_{dc}$ ) goes up. As  $V_{dc}$  goes up, the peak controlled secondary voltage will go up and after a delay in  $L_o$ ,  $V_o$  will eventually go up. Since secondary DC voltages are proportional to secondary winding peak voltages and power transistor “on” time, the “on” time must decrease because the peak secondary voltage has increased. Then, after a delay through the error amplifier,  $V_{eao}$  will go down and, in the PWM comparator, the ramp in  $V_i$  will become equal to the lowered value of  $V_{eao}$  earlier in time. Thus, “on” time will be decreased and the output voltage will be brought back down.

If this were the only mechanism to correct against line voltage changes, however, the correction would be slow due to the delays in

## 172 Switching Power Supply Design

$L_o$  and the error amplifier, but there is a shortcut around those delays. As  $V_{dc}$  goes up, the peak voltage at the input to the output inductor  $V_{sp}$  increases, the slope of inductor current  $DI_s/dt$  increases, and hence the slope of the ramp of  $V_i$  increases. Now the faster ramp equals  $V_{eao}$  earlier in time, and the “on” time is shortened without having to wait for  $V_{eao}$  to move down and shorten the “on” time. Output voltage transients resulting from input voltage transients are smaller in amplitude and shorter in duration because of this feed-forward characteristic.

### 5.4.2 Elimination of Flux Imbalance

Consider the waveform  $V_i$  in Figure 5.3. It is taken from the current-sensing resistor  $R_i$  and is hence proportional to power transistor currents. The “on” time ends when the peak of the ramp in  $V_i$  equals the output voltage of the error amplifier  $V_{eao}$ . It can be seen in Figure 5.3 that peak currents on alternate half cycles cannot be unequal as in Figure 2.4*b* and 2.4*c* because the error-amplifier output  $V_{eao}$  is essentially horizontal and cannot change significantly within one cycle because of limited EA bandwidth.

If the transformer core got slightly off center and started walking up into saturation on one side, the voltage  $V_i$  would become slightly concave upward close to the end of that “on” time. It would then equal  $V_{eao}$  earlier and terminate that “on” time sooner. Flux increase in that half cycle would then cease, and in the next half cycle, since the opposite transistor would not have a foreshortened “on” time, the core flux would be brought back down and away from saturation.

Since the peaks of the voltage ramps in Figure 5.3 ( $V_i$ ) are equal, peak currents on alternate half cycles must be equal. Thus the inequality of alternate currents and flux imbalance shown in Figure 2.4*b* are not possible.

### 5.4.3 Simplified Loop Stabilization from Elimination of Output Inductor in Small-Signal Analysis

Refer to Figure 5.3. In a small-signal analysis to determine whether the outer voltage loop is stable, it is assumed that the loop is opened at some point and a small sinusoidal signal of variable frequency is inserted at the input side of the break. The gain and phase shift versus frequency are calculated through all the loop elements starting from the input side of the break, around to the same point at the output side of the loop break. By tailoring the error-amplifier gain and phase shift properly in relation to the other elements in the open loop (primarily the output  $LC$  filter), the closed loop is made stable.

The variable frequency is often inserted at the input to the error amplifier. In Chapter 12 on feedback loop stability analysis, it will be shown how gain and phase shift through the error amplifier may be calculated and tailored to achieve the desired results.

Considering Figure 5.3, the concept of gain and phase shift of a sinusoidal signal from the error-amplifier output to the input of the  $LC$  filter may not be obvious. Of primary importance is the fact that the highest frequency to which the loop will respond significantly is well below the switching frequency of the converter. The error-amplifier output  $V_{eao}$  is, therefore, a slowly changing or essentially DC voltage that, when it equals the peak of the ramp-on-a-step pulse sequence  $V_i$ , results in a sequence of negative-going pulses at  $Q_{pw}$  whose duration depends on  $V_{eao}$ . The  $Q_{pw}$  negative pulses result in a sequence of positive-going pulses at the input to the  $LC$  filter.

It may seem puzzling to speak of gain and phase shift of sinusoidal signals in view of this odd operation of converting a voltage level to a sequence of pulses at the switching frequency. The situation may be clarified as follows.

If there is a sinusoidal signal at the error-amplifier input, it is amplified and phase-shifted at the EA output. Thus  $V_{eao}$  is sinusoidally amplitude modulated at that frequency. The  $Q_{pw}$  negative pulses are similarly pulse width modulated at that frequency. So are the “on” times of the positive-going pulses at the output rectifiers pulse width modulated at that frequency. Hence, the voltage at the output rectifier cathodes, which is proportional to the pulse widths, when averaged over a time long compared to the switching period, is simply amplitude modulated at the same frequency as was inserted at the error-amplifier input.

So long as the modulation period is long compared to the switching period, the modulation operation is a sinusoid-to-pulse width-to-sinusoid converter. The gain of this modulation operation will be discussed further in the chapter on feedback loop stability.

In the converter of Figure 5.3, there remains only the problem of calculating the gain and phase shift versus frequency for the sinusoid through the  $LC$  filter. A sine wave voltage at the rectifier cathodes will be phase shifted  $90^\circ$  by the  $LC$  filter at the resonant frequency  $\frac{1}{2\pi\sqrt{LC}}$  and  $180^\circ$  at frequencies above that, and gain from input to output will fall at  $-40$  dB/decade above resonance.

In current mode, however, the PWM comparator forces the output at the rectifier cathodes to be a sequence of width-modulated constant-current pulses—not voltage pulses. Thus at the input to the  $LC$  filter, the averaged waveform is a constant-current, not a constant-voltage, sinusoid.

With a constant-current sinusoid, the filter inductor cannot act to change phase. The circuit behaves, in this small-signal analysis, as if

## 174 Switching Power Supply Design

the inductor were not present. Thus after the rectifier cathodes, the gain and phase shift correspond to that of a constant-current sinusoid flowing into the parallel combination of the output capacitor and load resistor. Such a circuit can yield a maximum phase shift of only  $90^\circ$ , and a gain-versus-frequency characteristic that falls at  $-20$  dB per decade, rather than  $-40$  dB.

Chapter 12 on feedback stability analysis will show that this greatly simplifies the error-amplifier design, yields greater bandwidth, and improves the response of the closed-loop circuit to step changes in load current and line voltage. For now, Figure 5.4a and 5.4b show a comparison of the error-amplifier feedback networks required to stabilize a voltage-mode circuit (Figure 5.4a) and a current-mode circuit (Figure 5.4b).

**After Pressman** *Notice the inductor is only taken out of the loop for small signal changes (it is still there in fact). For larger transient changes, the inductor will still limit the slew rate and cannot be ignored for large changes (where the control amplifiers bottom or top out at the limit of their range). ~K.B.*

### 5.4.4 Load Current Regulation

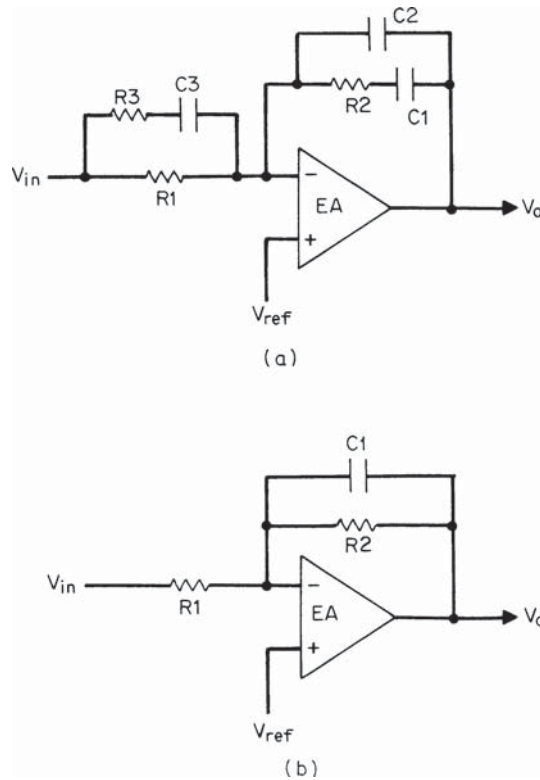
In Figure 5.3, the  $V_i$  voltage waveform is proportional to power transistor currents, which are related to controlled secondary current by the transformer turns ratio.

At a DC input voltage  $V_{dc}$ , the peak secondary voltage is  $V_{sp} = V_{dc}(N_s/N_p)$ . For an “on” time of  $t_{on}$  in each transistor, the DC output voltage is  $V_o = V_{sp}(2t_{on}/T)$ —just as for a voltage-mode push-pull circuit. The “on” time starts at the clock pulse, as shown in Figure 5.3, and ends when the  $V_i$  ramp equals the voltage error-amplifier output.

If the DC voltage goes up as described, initially the  $V_i$  ramp rate increases and shortens the “on” time as it reaches the original  $V_{eao}$  level earlier in time. This yields a fast correction for a step change in input voltage and the “on” time remains shorter as required by the preceding relation for the increase in peak secondary voltage.

The mechanism for load current regulation, though, is different. For a fast step increase—say—in DC load current, the DC output voltage drops momentarily somewhat because the  $LC$  output filter has a surge impedance of approximately  $\sqrt{LC}$ . After the delay in the error amplifier,  $V_{eao}$  moves up an amount determined by the EA gain.

Now  $V_i$  must ramp longer and hence higher in amplitude for it to reach equality with the higher  $V_{eao}$ . The secondary peak current and hence the output inductor current are thus larger in amplitude. The up-slope of the inductor current lasts longer and eats somewhat into the dead time before the opposite transistor turns “on.”



**FIGURE 5.4** (a) Typical compensating network for a voltage-mode power supply. The complex input-feedback network in voltage mode is necessary because the output inductor with the filter capacitor together yields a  $180^\circ$  phase shift and a  $-40$  dB/decade gain versus frequency characteristic, which make loop stabilization more difficult. (b) Typical compensation network for a current-mode power supply. In current mode, the source driving the output inductor is an effective “current source.” The output inductor does not contribute to phase shift. The circuit acts at its output as if there were a constant current driving the parallel combination of the output filter capacitor and the output load resistance. Such a network yields a maximum  $90^\circ$  phase shift and a  $-20$  dB/decade gain versus frequency characteristic. This permits the simpler input-feedback network for loop stabilization. It also copes much more easily with large-amplitude load and line changes.

With a shorter dead time, when the opposite transistor turns “on” at the beginning of the dead time, the current remaining in the inductor will be greater than it had been in the previous cycle. Thus the front-end step in each current pulse represented by  $V_i$  will be greater than that in the previous cycle.

## 176 Switching Power Supply Design

This process continues for a number of switching cycles, until the step part of the ramp-on-a-step current waveform builds up sufficiently to supply the increased demand for DC load current. As this current builds up, the DC output voltage gradually builds back up and  $V_{eao}$  relaxes back down, returning the “on” time to its original value. The time to respond to a change in DC load current is thus seen to be dependent on the size of the output inductor, since a smaller value permits more rapid current changes. The response time also depends on the bandwidth of the error amplifier.

### 5.5 Current-Mode Deficiencies and Limitations

#### 5.5.1 Constant Peak Current vs. Average Output Current Ratio Problem<sup>1-4</sup>

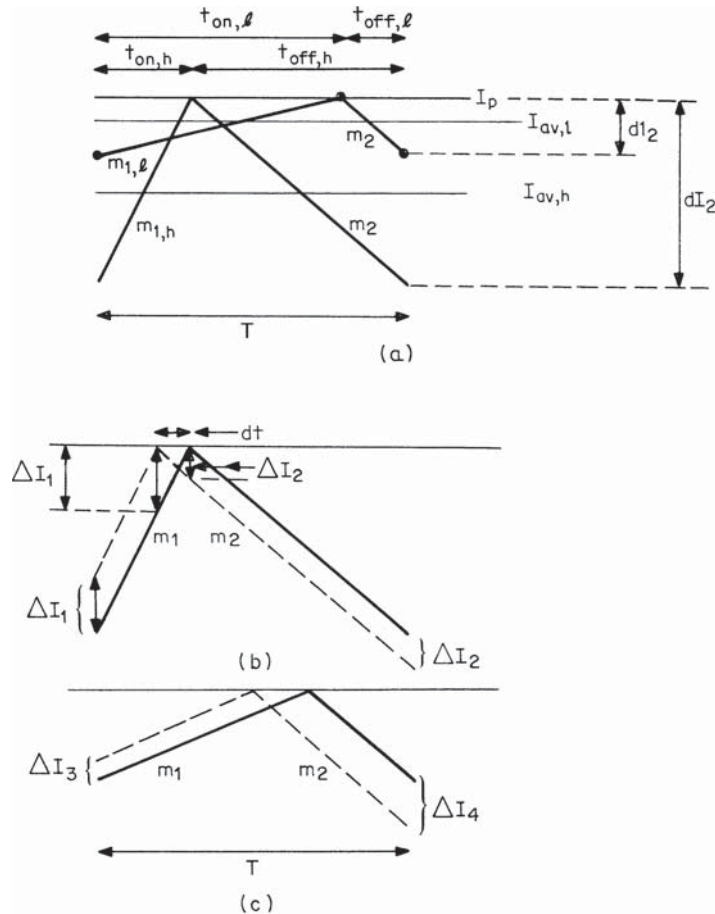
Current mode controls the peak transistor currents (and hence the peak output inductor/choke currents) constant at a level needed to supply the required mean DC load current to give the mean DC output voltage dictated by the voltage error amplifier, as shown in Figure 5.3.

The DC load current is the average of the output inductor current so that keeping the peak transistor current constant, and hence the peak output inductor current constant, does not keep the average inductor current and hence output current constant. Because of this, in the unmodified current-mode scheme described thus far, changes in the DC input voltage will cause momentary changes in the DC output voltage. After a short delay the output voltage change will be corrected by the voltage error amplifier in the outer feedback loop, as this is the loop that ultimately sets output voltage.

**After Pressman** *This is now referred to as the “peak to average current ratio” effect. The problem stems from the fact that maintaining the peak inductor current constant does not maintain the average output current constant, because duty cycle changes change the average value but not the peak value. This can become a problem for wide duty cycle changes, leading to sub-harmonic instability. It is corrected by ramp compensation (Section 5.5.3). ~K.B.*

However, the inner loop, in keeping peak inductor current constant, does not supply the correct average inductor current and output voltage changes again. The effect is an oscillation that commences at every change in input voltage and that may continue for some time. The mechanism can be better understood from an examination of the up- and down-slopes of the output inductor currents in Figure 5.5.<sup>3</sup>





**FIGURE 5.5** Problems in current mode. (a) Output inductor currents at high and low input voltages. In current mode, peak inductor currents are constant. At low DC input,  $t_{on}$  is maximum, yielding average inductor current  $I_{av,l}$ . At high DC input, "on" time decreases to keep output voltage constant. But average inductor current  $I_{av,h}$  is lower at high DC input. Since output voltage is proportional to average—not peak—inductor current, this causes oscillation when input voltage is changed. Slope  $m_2$  is inductor current down-slope, which is not affected by loop action and is constant. Slope  $m_{1l}$  is inductor current up-slope at low line;  $m_{1h}$  is inductor current up-slope at high line. (b) For a duty cycle less than 50%, an initial inductor current disturbance  $I_1$  results in smaller  $I_2$  disturbances in successive cycles until the disturbances die out. (c) For a duty cycle greater than 50%, an initial inductor current disturbance  $I_3$  results in larger  $I_4$  disturbances in successive cycles. The disturbances grow and then decay, resulting in an oscillation.



## 178 Switching Power Supply Design

Figure 5.5a shows the up- and down-slopes of the output inductor current for two different DC input voltages in current mode. Slope  $m_2$  is the down-slope  $= dI_1/dt = V_o/L_o$ . It is seen to be constant for the two different DC input voltages. At the high input voltage, “on” time is short at  $t_{on,h}$  and at the lower DC input, “on” time is longer at  $t_{on,l}$ .

The peak inductor currents are constant because the power transistor peak currents are kept constant by the PWM comparator (see Figure 5.3). The DC voltage input  $V_{eao}$  to that comparator is constant since the outer feedback loop is keeping  $V_o$  constant. The constant  $V_{eao}$  then keeps  $V_i$  peaks constant, and hence transistor and output inductor peak currents are constant.

In Figure 5.5a, in the steady state, the current change in the output inductor during an “on” time is equal and opposite to that during an “off” time. If this were not so, there would be a DC voltage across the inductor, and since it is assumed that the inductor has negligible resistance, it cannot support DC voltage.

It can be seen in Figure 5.5a that the average inductor current at low DC input is higher than it is at high DC input voltage. This can be seen quantitatively as

$$\begin{aligned}
 I_{av} &= I_p - \frac{dI_2}{2} \\
 &= I_p - \left( \frac{m_2 t_{off}}{2} \right) \\
 &= I_p - \left[ \frac{m_2 (T - t_{on})}{2} \right] \\
 &= I_p - \left( \frac{m_2 T}{2} \right) + \left( \frac{m_2 t_{on}}{2} \right) \quad (5.1)
 \end{aligned}$$

Since the voltage feedback loop keeps the product of  $V_{dc} t_{on}$  constant, at lower DC input voltage when the “on” time is higher, the average output inductor current  $I_{av}$  is higher, as can be seen from Eq. 5.1 and Figure 5.5a.

Further, since the DC output voltage is proportional to the average and not the peak inductor current, as DC input goes down, DC output voltage will go up. DC output voltage will then be corrected by the outer feedback loop and a seesaw action or oscillation will occur.

This phenomenon does not occur in voltage-mode control, in which only DC output voltage is controlled. Also, since DC output voltage is proportional to average and not peak inductor current, keeping output voltage constant maintains average inductor current constant.

### 5.5.2 Response to an Output Inductor Current Disturbance

A second problem that gives rise to oscillation in current mode is shown in Figure 5.5b and 5.5c. In Figure 5.5b, it is seen that at a fixed DC input voltage, if for some reason there is an initial current disturbance  $\Delta I_1$ , after a first down-slope the current will be displaced by an amount  $\Delta I_2$ .

Further, if the duty cycle is less than 50% ( $m_2 < m_1$ ), as in Figure 5.5b, the output disturbance  $\Delta I_2$  will be less than the input disturbance  $\Delta I_1$ , and after a few cycles, the disturbance will die out. If the duty cycle is greater than 50% ( $m_2 > m_1$ ) as in Figure 5.5c, the output disturbance  $\Delta I_4$  after one cycle is greater than the input disturbance  $\Delta I_3$ . This can be seen quantitatively from Figure 5.5b as follows. For a small current displacement  $\Delta I_1$ , the current reaches the original peak value earlier in time by an amount  $dt$  where  $dt = \Delta I_1 / m_1$ .

On the inductor down-slope, at the end of the “on” time, the current is lower than its original value by an amount  $\Delta I_2$  where

$$\Delta I_2 = m_2 dt = \Delta I_1 \frac{m_2}{m_1} \quad (5.2)$$

Now with  $m_2$  greater than  $m_1$ , the disturbances will continue to grow but eventually decay, giving rise to an oscillation.

### 5.5.3 Slope Compensation to Correct Problems in Current Mode<sup>1-4</sup>

Both current-mode problems mentioned above can be corrected as shown in Figure 5.6, in which the original, unmodified output of the error amplifier is shown as the horizontal voltage level  $OP$ . The “slope compensation” scheme for correcting the preceding problems consists of adding a negative voltage slope of magnitude  $m$  to the output of the error amplifier. By proper selection of  $m$  in a manner discussed below, the output inductor average DC current can be made independent of the power transistor “on” time. This corrects the problems indicated by both Eqs. 5.1 and 5.2.

In Figure 5.6, the up-slope  $m_1$  and down-slope  $m_2$  of output inductor current are shown. Recall that in current mode, the power transistor “on” time starts at every clock pulse and ends at the instant the output of the PWM comparator reaches equality with the output of the voltage error-amplifier as shown in Figure 5.3. In slope compensation, a negative voltage slope of magnitude  $m = dV_{ea}/dt$  starting at clock time is added to the error-amplifier output. The magnitude of  $m$  is calculated thus: In Figure 5.6, the error-amplifier output at any time

## 180 Switching Power Supply Design

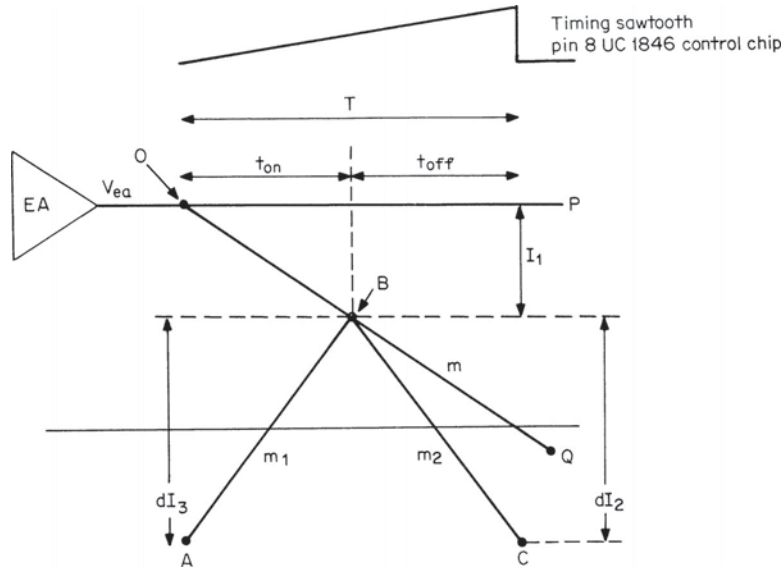


FIGURE 5.6 Slope compensation. By adding a negative voltage slope of magnitude  $m = N_s/N_p(R_i)(m_2/2)$  to the error-amplifier output (Figure 5.3), the two problems shown in Figure 5.5 are corrected.

$t_{on}$  after a clock pulse is

$$V_{ea} = V_{eao} - mt_{on} \quad (5.3)$$

where  $V_{eao}$  is the error-amplifier output at clock time. The peak voltage  $V_i$  across the primary current-sensing resistor  $R_i$  in Figure 5.3 is

$$V_i = I_{pp}R_i = I_{sp} \frac{N_s}{N_p} R_i$$

in which  $I_{pp}$  and  $I_{sp}$  are the primary and secondary peak currents, respectively. But  $I_{sp} = I_{sa} + dI_2/2$ , where  $I_{sa}$  is the average secondary or average output inductor current and  $dI_2$  in Figure 5.6 is the inductor current change during the "off" time ( $= m_2 t_{off}$ ). Then

$$\begin{aligned} I_{sp} &= I_{sa} + \frac{m_2 t_{off}}{2} \\ &= I_{sa} + \frac{m_2}{2} (T - t_{on}) \end{aligned}$$

$$\text{So} \quad V_i = \frac{N_s}{N_p} R_i \left[ I_{sa} + \frac{m_2}{2} (T - t_{on}) \right] \quad (5.4)$$

Equating Eqs. 5.3 and 5.4, which is what the PWM comparator does, we obtain

$$\frac{N_s}{N_p} R_i I_{sa} = V_{eao} + t_{on} \left( \frac{N_s}{N_p} R_i \frac{m_2}{2} - m \right) - \left( \frac{N_s}{N_p} R_i \frac{m_2}{2} T \right)$$

It can be seen in this relation that if

$$\frac{N_s}{N_p} R_i \frac{m_2}{2} = m = \frac{dV_{ea}}{dt} \quad (5.5)$$

then the coefficient of the  $t_{on}$  term is zero and the average output inductor current is independent of the “on” time. This then corrects the above two problems arising from the fact that without compensation, current mode maintains the peak, and not the average, output inductor current constant.

### 5.5.4 Slope (Ramp) Compensation with a Positive-Going Ramp Voltage<sup>3</sup>

In the previous section it was shown that if a negative ramp of magnitude given by Eq. 5.5 is added to the error-amplifier output, the two current-mode problems described above are corrected.

The same effect is obtained by adding a positive-going ramp to the output of the current-sensing resistor  $V_i$  (Figure 5.3) and leaving the error-amplifier output voltage  $V_{eao}$  (Figure 5.3) unmodified. Adding a positive ramp to  $V_i$  is simpler and is the more usual approach. That adding the appropriate positive ramp to  $V_i$  also makes the average output inductor current independent of “on” time can be shown as follows: A ramp voltage of slope  $dV/dt$  will be added to the voltage  $V_i$  of Figure 5.3, and the resultant voltage will be compared in the PWM to the error-amplifier output  $V_{eao}$  of that figure. When the PWM finds equality of those voltages, its output terminates the “on” time. Then  $V_i + dV/dt = V_{eao}$ . Substitute  $V_i$  from Eq. 5.4:

$$\frac{N_s}{N_p} R_i \left[ I_{sa} + \frac{m_2}{2} (T - t_{on}) \right] + \frac{dV}{dt} t_{on} = V_{eao}$$

Then

$$\frac{N_s}{N_p} R_i I_{sa} + \frac{N_s}{N_p} R_i \frac{m_2}{2} T + t_{on} \left( \frac{dV}{dt} - \frac{N_s}{N_p} R_i \frac{m_2}{2} \right) = V_{eao}$$

From the above, it is seen that if the slope  $dV/dt$  of the voltage added to  $V_i$  is equal to  $(N_s/N_p) R_i m_2/2$ , the terms involving  $t_{on}$  in the preceding relation vanish and the secondary average voltage  $I_{sa}$  is independent of the “on” time. Note that  $m_2 (= V_o/L_o)$  is the current down-slope of the output inductor as defined earlier.

## 182 Switching Power Supply Design

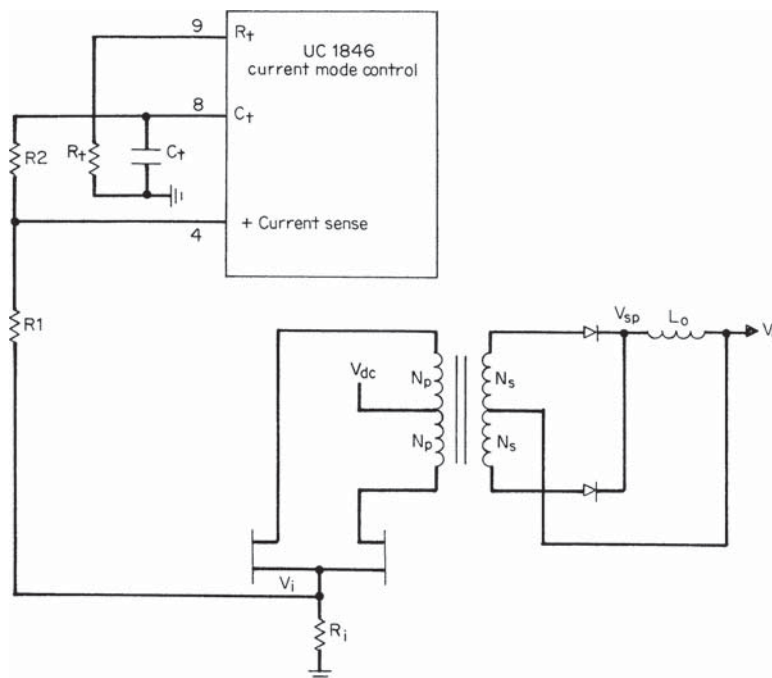
### 5.5.5 Implementing Slope Compensation<sup>3</sup>

In the UC1846 chip, a positive-going ramp starting at every clock pulse is available across the timing capacitor (pin 8 in Figure 5.2b). The voltage at that pin is

$$V_{osc} = \frac{\Delta V}{\Delta t} t_{on} \quad (5.6)$$

where  $\Delta V = 1.8 \text{ V}$  and  $\Delta t = 0.45 R_t C_t$ .

As seen in Figure 5.7, a fraction of that voltage, whose slope is  $\Delta V/\Delta t$ , is added to  $V_i$  (the voltage across the current-sensing resistor).



**FIGURE 5.7** Slope compensation in the UC1846 current-mode control chip. A positive ramp voltage is taken from the timing capacitor, scaled by resistors  $R_1$ ,  $R_2$  and added to the voltage on the current resistor  $R_i$ . By choosing  $R_1$ ,  $R_2$  to make the slope of the voltage added to  $V_i$  equal to half the down-slope of the output inductor current reflected into the primary and multiplied by  $R_i$ , the average output inductor current is rendered independent of power transistor "on" times.

That slope is set to  $(N_s/N_p)R_i(m_2/2)$  by resistors  $R_1$ ,  $R_2$ . Thus in Figure 5.7, since  $R_i$  is much less than  $R_1$ , the voltage delivered to the current-sensing terminal (pin 4) is

$$V_i + \frac{R_1}{R_1 + R_2} V_{\text{osc}} = V_i + \frac{R_1}{R_1 + R_2} \frac{\Delta V}{\Delta t} t_{\text{on}} \quad (5.7)$$

and setting the slope of that added voltage equal to  $(N_s/N_p)R_i m_2/2$ , we obtain

$$\frac{R_1}{R_1 + R_2} = \frac{(N_s/N_p)(R_i)(m_2/2)}{\Delta V/\Delta t} \quad (5.8)$$

in which  $\Delta V/\Delta t = 1.8/(0.45R_t C_t)$ .

Since  $R_1 + R_2$  drains current from the timing capacitor, they change operating frequency. Then either  $R_1 + R_2$  is made large enough so that the frequency change is small, or a buffer amplifier is interposed between pin 8 and the resistors. Usually  $R_1$  is preselected and  $R_2$  is calculated from Eq. 5.8.

**After Pressman** *With large values of inductance  $L_o$  or at higher frequencies, the slope on the current waveform (Figure 5.5) as it approaches the point of transition to the "off" state can approach zero. Hence any small noise spike can cause early or late switching resulting in jitter and noise in the output. In effect, the gain of the fast current control loop becomes very high. Close attention to layout and using a non-inductive current-sensing resistor for  $R_i$  or a DCCT may help. But in many cases the solution requires a reduction in inductance resulting in an increase in high frequency ripple current. ~K.B.*

## 5.6 Comparing the Properties of Voltage-Fed and Current-Fed Topologies

### 5.6.1 Introduction and Definitions

All topologies discussed thus far have been of the voltage-fed type. *Voltage-fed* implies that the source impedance of whatever drives the topology is low and hence there is no way of limiting the current drawn from it during unusual conditions at power switch turn "on" or turn "off," or under various fault conditions in the topology.

There are various ways of implementing "current limiting" with additional circuitry, which senses an over-current condition and takes some kind of corrective action such as narrowing the controller's switching pulse width or stopping it completely. But all such schemes are not instantaneous; they involve a delay over a number of switching cycles during which there can be excessive dissipation in either the power transistors or output rectifiers and dangerous voltage or

## 184 Switching Power Supply Design

current spiking. Thus such over-current sensing schemes are of no help in the case of high transient currents at the instant of the power switch turn “on” and turn “off.”

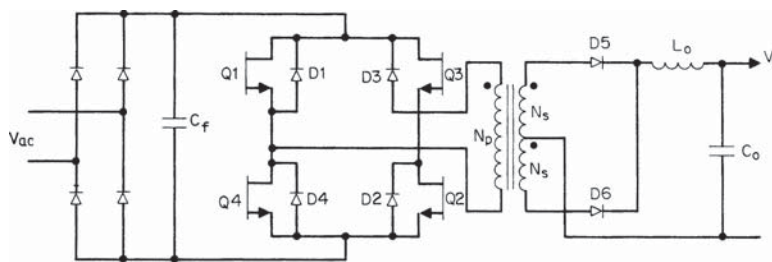
The low-source impedance in voltage-fed topologies is that of the filter capacitor in offline converters or of the battery in battery-powered converters. In compound schemes that use a buck regulator to preregulate the rectified DC voltage of the AC line rectifier, it is the very low-output impedance of the buck regulator itself.

In current-fed topologies, the high instantaneous impedance of an inductor is interposed between the power source and the topology itself. This provides a number of significant advantages, especially in high power supplies ( $> 1000\text{ W}$ ), high output voltage supplies ( $> 200\text{ V}$ ), and multi-output supplies where close tracking between slaves and a master output voltage is required.

Advantages of the current-fed technique can be appreciated by examining the usual shortcomings of high-power, high-output-voltage, and multi-output voltage-fed topologies.

### 5.6.2 Deficiencies of Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge<sup>9</sup>

Figure 5.8 shows a conventional voltage-fed full bridge—the usual choice for a switching supply at 1000-W output. At higher output powers, high output voltages, or multiple output voltages, it has the following significant shortcomings.



**FIGURE 5.8** A conventional voltage-fed full bridge, often used for higher output powers typically 1000 W or more. The low-source impedance of the filter capacitor  $C_f$  and the need for the output inductor  $L_o$  are significant drawbacks for output powers over 1000 W and output voltages over a few hundred volts. Further, in a multi-output power supply, the requirement for an output inductor at each output makes the topology expensive in cost and space.

### 5.6.2.1 Output Inductor Problems in Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge

For high-output voltages, the size and cost of the output inductor  $L_o$  (or inductors in a multi-output supply) becomes prohibitive as can be seen from the following. The inductor is selected to prevent going into the discontinuous mode or running dry at the specified minimum DC load current (Sections 1.3.6 and 2.2.14.1). For a minimum DC load current of one-tenth the nominal  $I_{on}$ , Eq. 2.20 gives the magnitude of the inductor as  $L_o = 0.5V_o T / I_{on}$ .

Now consider a 2000-W supply at  $V_o = 200$  V,  $I_{o(nominal)} = 10$  A, and a minimum DC output current of 1 A. To minimize the size of the output inductor,  $T$  should be minimized, and a switching frequency of 50 kHz might be considered. At 50 kHz, for  $V_o = 200$  V,  $I_{on} = 10$  A, Eq. 2.20 yields  $L_o$  of 200  $\mu$ H.

The inductor must carry the nominal current of 10 A without saturating. Inductors capable of carrying large DC bias currents without saturating are discussed in a later chapter and are made either with gapped ferrite or powdered iron toroidal cores. A 200- $\mu$ H 10-A inductor using a powdered iron toroid would have a diameter about 2.5 in and a height about 1.0 in.

Although this is not a prohibitive size for a single-output 2-kW supply, a supply with many outputs, higher output voltage, or higher output power, the size and cost of many large inductors would be a serious drawback. For high-output voltages ( $> 1000$  V), even at low-output currents, the output inductor is far more troublesome because of the large number of turns required to support the high voltage across the inductor. This high voltage—especially during the dead time when cathodes of  $D5$ ,  $D6$  of Figure 5.8 are both “low”—can produce corona and arcing.

A further problem with a topology requiring output inductors, as shown in Figure 5.8, is the poor cross regulation or change in output voltage of a slave when current changes in the master (Section 2.2.2). The output inductors in both the master and slave must be large enough to prevent discontinuous mode operation and large-output voltage changes at minimum load currents.

The current-fed topology (Figure 5.10) discussed below avoids many of the above problems, as it does not require multiple output inductors. It uses a single input inductor  $L1$  in place of the individual output inductors, and is positioned before the high frequency switching bridge circuit and after line rectification and storage capacitors. Thus DC output voltages are the peak rather than the average of the transformer secondary voltages. Voltage regulation is achieved by pulse-width modulation of the bridge, or as in Figure 5.10, by a buck regulator transistor switch  $Q5$  ahead of the  $L1$  inductor.



## 186 Switching Power Supply Design

**5.6.2.2 Turn “On” Transient Problems in Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge<sup>9</sup>**

In Figure 5.8, diagonally opposite transistors are simultaneously “on” during alternate half cycles. The maximum “on” time of each pair is designed to be less than 80% of a half period. This ensures a  $0.2T/2$  dead time between the turn “off” of one transistor pair and the turn “on” of the other. This dead time is essential, for if the “on” time of alternate pairs overlapped by even a fraction of a microsecond, there would be a dead short circuit across the filter capacitor, and with nothing to limit current flow, the transistors would fail immediately.

During the dead time, all four transistors are “off,” the anodes of output rectifiers  $D5$ ,  $D6$  are at zero volts, and the voltage at the input end of filter inductor  $L_o$  has swung down to keep the current constant. The input end of  $L_o$  is clamped at one diode drop below ground by  $D5$ ,  $D6$ , which act as free-wheeling diodes. The current that had been flowing in  $L_o$  before the dead time (roughly equal to the DC output current) continues to flow in the same direction. It flows out through the ground terminal into the secondary center tap, where it divides equally with half flowing through each of  $D5$  and  $D6$  and back into the input end of  $L_o$ .

At the start of the next half cycle when, say,  $Q1$ ,  $Q2$  turn “on,” the no-dot end of the  $T1$  primary is high and the no-dot end of the  $T1$  secondary (anode of  $D6$ ) attempts to go high. But the cathode of  $D6$  is looking into the cathode of  $D5$ , which is still conducting half the DC output current. Until  $D6$  supplies a current equal to and canceling the  $D5$  forward current, it is looking into the low impedance of a conducting diode ( $\sim 10 \Omega$ ).

This low secondary impedance reflects as a low impedance across the primary. But this low impedance is in series with the transformer’s leakage inductance, which limits the primary current during the time required to cancel the  $D5$  free-wheeling current. Because of the high-impedance current-limiting effect of the leakage inductance, transistors  $Q1$  and  $Q2$  remain in saturation until the  $D5$  free-wheeling current is canceled.

When the  $D5$  current is canceled, it still has a low impedance because of its reverse-recovery time, which may range from 35 ns (ultra-fast-recovery type) to 200 ns (fast-recovery type). For a reverse-recovery time of  $t_r$ , supply voltage of  $V_{cc}$ , and transformer primary leakage inductance of  $L_l$ , the primary current overshoots to  $V_{cc}t_r/L_l$ . This overshoot current can pull the transistors out of saturation and either damage or destroy them.

Finally, when the output rectifier recovers abruptly, there is a damped oscillatory ring at its cathode. The first positive half cycle of this ring can more than double the reverse voltage stress on the diode and possibly destroy it. Even in lower power supplies, it is often

necessary to put series RC snubbers across the rectifiers to damp the oscillation. The penalty paid for this is, of course, dissipation in the resistors.

### 5.6.2.3 Turn “Off” Transient Problems in Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge<sup>9</sup>

In Figure 5.8, there is a spike of high power dissipation at turn “off” as a result of the instantaneous overlap of falling current and rising voltage across the “off”-turning transistors.

Consider that  $Q3$  and  $Q4$  are “on” and have received turn “off” signals at their bases. As  $Q3$ ,  $Q4$  commence turning “off,” current stored in the leakage and magnetizing inductance of  $T1$  force a polarity reversal across the primary. The bottom end of  $T1$  primary goes immediately positive and is clamped via  $D1$  to the positive rail at the top of  $C_f$ . The top end of  $T1$  primary goes immediately negative and is clamped via  $D2$  to the negative rail at the bottom end of  $C_f$ . Now voltages across  $Q3$  and  $Q4$  are clamped at  $V_{cc}$  so long as diodes  $D1$ ,  $D2$  conduct. There are no leakage inductance voltage spikes across  $Q3$ ,  $Q4$  as in push-pull or single-ended forward converter topologies. Energy stored in the leakage inductance is returned without dissipation to the input capacitor  $C_f$ .

However, while the voltage across  $Q3$ ,  $Q4$  is held at  $V_{cc}$ , the current in these two transistors falls linearly to zero in a time  $t_f$  determined by their reverse base drives. This overlap of a fixed-voltage  $V_{cc}$  and a current falling linearly from a value  $I_p$  results in dissipation averaged over a full period  $T$  of

$$PD = V_{cc} \frac{I_p}{2} \frac{t_f}{T} \quad (5.9)$$

It is instructive to calculate this dissipation for, say, a 2-kW supply operating at 50 kHz from a nominal  $V_{cc}$  of 336 V (typical  $V_{cc}$  for an offline inverter operating from a 120-V AC line in the voltage-doubling mode as in Section 3.1.1). Assume a minimum  $V_{cc}$  of 0.9 (336 V) or 302 V. Then from Eq. 3.7, the peak current is

$$I_p = \frac{1.56 P_o}{V_{dc}} = 1.56 \frac{2000}{302} = 10.3 \text{ A}$$

A bipolar transistor at this current has a fall time of perhaps 0.3  $\mu$ s. Since peak currents are independent of DC input voltage, calculate overlap dissipation from Eq. 5.9 at a high line of  $1.1 \times 336 = 370$  V. For the dissipation in either  $Q3$  or  $Q4$ , Eq. 5.9 gives  $PD = V_{cc}(I_p/2)(t_f/T) = 370(10.3/2)(0.3/20) = 28.5$  W, and for the four transistors in the bridge, total overlap losses would be 114 W.

## 188 Switching Power Supply Design

It is of interest to calculate the dissipation per transistor during the “on” time. This is  $V_{ce(sat)} I_c T_{on}/T$  and for a typical  $V_{ce(sat)}$  of 1.0 V and an “on” duty cycle of 0.4 is only  $1 \times 10.3 \times 0.4$  or 4.1 W.

Even though the 28.5 W of overlap dissipation per transistor can be reduced with four load- and line-shaping “snubbers” (to be discussed in a later chapter), these snubbers reduce transistor losses only by diverting them to the snubber resistors with no improvement in efficiency. It will be shown that in the current-fed topology, only two snubbers will be required, reducing transistor overlap dissipation to a negligible value. The price paid for this is the dissipation in each of the two snubber resistors of somewhat more than that in the voltage-fed full bridge.

### 5.6.2.4 Flux-Imbalance Problem in Voltage-Fed, Pulse-Width-Modulated Full-Wave Bridge

Flux imbalance, or operation not centered about the origin of the transformer’s  $BH$  loop, was discussed in Section 2.2.5 in connection with the push-pull and in Section 3.2.4 for the half bridge. It arises because of unequal volt-second products applied to the transformer primary on alternate half cycles. As the core drifts farther and farther off center on the  $BH$  loop, it can move into saturation where it is unable to sustain the supply voltage and destroy the transistor.

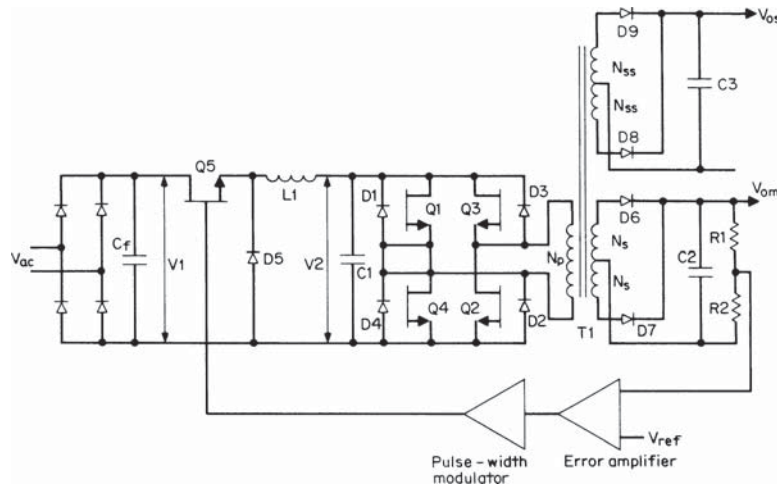
Flux imbalance can also arise in the conventional full-wave bridge because of a volt-second imbalance on alternate half cycles. This can come about with bipolar transistors because of unequal storage times on alternate half cycles or with MOSFET transistors because of unequal MOSFET “on”-voltage drops. The solution for the full-wave bridge is to place a DC blocking capacitor in series with the primary. This prevents a DC current bias in the primary and forces operation to be centered about the  $BH$  loop origin. The size of such a DC blocking capacitor is calculated as in Section 3.2.4 for the half bridge.

The current-fed circuits, discussed below, do not require DC blocking capacitors, providing another advantage over voltage-fed circuits. This is still an advantage despite the relatively small size and cost of such blocking capacitors.

### 5.6.3 Buck Voltage-Fed Full-Wave Bridge Topology—Basic Operation

This topology is shown in Figure 5.9. It avoids many of the deficiencies of the voltage-fed pulse-width-modulated full-wave bridge in high-voltage, high-power, multi-output supplies.

Consider first how it works. There is a buck regulator preceding a square-wave inverter, which has only capacitors after the secondary



**FIGURE 5.9** Buck voltage-fed full bridge. The buck regulator preceding the full bridge eliminates the output inductors in a multi-output supply, but the low-source impedance of the buck capacitor and the low-output impedance of the buck regulator still leave many drawbacks to this approach. Q5 is pulse-width-modulated, but Q1 to Q4 are operated at a fixed “on” time at about 90% of a half period to avoid simultaneous conduction. The output filters C2, C3 are peak rather than averaging rectifiers. Practical output powers of about 2 kW to 5 kW are realizable.

rectifying diodes. Thus the DC output voltage at the filter capacitor is the peak of the secondary voltage less the negligible rectifying diode drop. Neglecting also the inverter transistor “on” drop, the DC output voltage is  $V_o = V_2(N_s/N_p)$ , where  $V_2$  is the output of the buck regulator. The inverter transistors are not pulse-width-modulated. They are operated at a fixed “on” time—roughly 90% of a half period to avoid simultaneous conduction in the two transistors positioned vertically one above another. Diagonally opposite transistors are switched “on” and “off” simultaneously.

Feedback is taken from one of the secondary outputs (usually the output with highest current or tightest output voltage tolerance) and used to pulse-width-modulate the buck transistor Q5. This bucks down the rectified, unregulated DC voltage  $V_1$  to a DC value  $V_2$ , which is usually selected to be about 25% lower than the lowest rectified voltage  $V_1$  corresponding to the lowest specified AC input voltage. The turns ratio  $N_s/N_p$  is then chosen so that for this value of  $V_2$ , the correct master output voltage  $V_{om} = V_2(N_s/N_p)$  is obtained.

## 190 Switching Power Supply Design

The feedback loop, in keeping  $V_{om}$  constant against line and load changes, then keeps  $V_2$  constant (neglecting relatively constant rectifier diode drops) at  $V_2 = V_o(N_p/N_s)$ . Additional secondaries, rectifier diodes, and peak-rectifying filter capacitors can be added for slave outputs.

Alternatively, feedback can be taken from C1 to keep  $V_2$  constant. From  $V_2$  to the outputs, the circuit is open-loop. But all output voltages are still quite insensitive to line and load changes because they change only slightly with forward drops in diode rectifiers and “on” drops of the transistors, which change only slightly with output currents. Thus the output voltages are all largely proportional to  $V_2$ .

Taking feedback from  $V_2$  results in somewhat less constant output voltage, but avoids the problem of transmitting a pulse-width-modulated control voltage pulse across the boundary from output to input common. If an error amplifier is located on output common with a pulse-width modulator on input common, it avoids the problem of transmitting the amplified DC error voltage across the output-input boundary. Such a scheme usually involves the use of an optocoupler, which has wide tolerances in gain and is not too reliable a device.

### 5.6.4 Buck Voltage-Fed Full-Wave Bridge Advantages

#### 5.6.4.1 Elimination of Output Inductors

The first obvious advantage of the topology for a multi-output supply is that it replaces many output inductors with a single input inductor with consequent savings in cost and space.

Since there are no output inductors in either the master or slaves, there is no problem with large output voltage changes that result from operating the inductors in discontinuous mode (Sections 1.3.6 and 2.2.4). Slave output voltages track the master over a large range of output currents, within about  $\pm 2\%$ , rather than the  $\pm 6$  to  $\pm 8\%$  with output inductors in continuous mode, or substantially more in discontinuous mode.

**After Pressman** *Providing the outputs share a common return, this problem can also be solved in the multiple output inductor case by using the coupled inductor approach. Here a single inductor has a winding for each output wound on a single core. The transformer type coupling between the windings also eliminates many of the problems shown above.*<sup>1</sup> ~K.B.

The input inductor is designed to operate in continuous mode at any current above the minimum. Since it is unlikely that all outputs are at minimum current simultaneously, this indicates a higher total minimum current and a smaller input inductor (Section 1.3.6).

Further, even if the input inductor goes discontinuous, the master output voltage will remain substantially constant, but with somewhat more output ripple and somewhat poorer load regulation. The feedback loop will keep the main output voltage constant even in discontinuous mode through large decreases in “on” time of the buck transistor (Figure 1.6a).

Further, since the slave outputs are clamped to the main output in the ratio of their respective turns ratios, slaves will also remain constant against large line and load changes.

Elimination of output inductors, with the many turns required to sustain high AC voltages for high voltage DC outputs, makes 2000- to 3000-V outputs easily feasible. Higher output voltages—15,000 to 30,000 V—at relatively low-output currents as for cathode-ray tubes, or high-voltage high-current outputs as for traveling-wave tubes, are easily obtained by conventional diode-capacitor voltage multipliers after the secondaries.<sup>8</sup>

#### 5.6.4.2 Elimination of Bridge Transistor Turn “On” Transients

With respect to the full-wave pulse-width-modulated bridge of Figure 5.8, Section 5.6.2.2 discussed turn “on” transient current stresses in the bridge transistors ( $Q1$  to  $Q4$ ), and excessive voltage stress in the rectifying diodes ( $D5$ ,  $D6$ ).

It was pointed out in Section 5.6.2.2 that these stresses arose because the rectifier diodes were also acting as free-wheeling diodes. At the instant of turn “on” of one diagonally opposite pair (say  $Q1$ ,  $Q2$ ),  $D6$  was still conducting as a free-wheeling diode. Until the forward current in  $D6$  was canceled, the impedance seen by  $Q1$ ,  $Q2$  was the leakage inductance of  $T1$  in series with the low forward impedance of  $D6$  reflected into the primary.

Subsequently, when  $Q1$ ,  $Q2$  forced a current into the primary sufficient to cancel the  $D6$  forward current, there was still a low impedance reflected into the primary because of reverse recovery time in  $D6$ . This caused a large primary current overshoot that overstressed  $Q1$ ,  $Q2$ . At the end of the recovery time, when the large secondary current overshoot terminated, it caused an oscillation and excessive voltage stress on  $D6$ .

This current overstress on the bridge transistors and voltage overstress on the output rectifiers does not occur with the buck voltage-fed topology of Figure 5.9. The inverter transistors are operated with a dead time ( $\sim 0.1T/2$ ) between the turn “off” of one pair of transistors and the turn “on” of the other pair.

During this dead time when none of the bridge transistors are “on,” no current flows in the output rectifiers and output load current is

## 192 Switching Power Supply Design

supplied from the filter capacitors alone. Thus at the start of the next half period, the “on”-turning rectifier diode is not loaded down with a conducting free-wheeling diode as in Figure 5.8. The opposite diode has long since ceased conducting; thus there is no current overstress in the bridge transistors, no recovery time problem in the rectifier diodes, and hence no overvoltage stress in them.

### 5.6.4.3 Decrease of Bridge Transistor Turn “Off” Dissipation

In Section 5.6.2.3, it was calculated that for a 2000-W supply operating from a nominal input of 120-V AC in the input voltage-doubling mode, the bridge dissipation is 28.5 W at maximum AC input for each of the four transistors in the voltage-fed, pulse-width-modulated bridge circuit of Figure 5.8.

In the buck voltage-fed, full-wave bridge (Figure 5.9), this dissipation is somewhat less. This is so because, even at maximum AC input, the “off”-turning bridge transistors are subjected to bucked-down voltage  $V_2$  (Figure 5.9) of about 0.75 times the minimum rectified voltage as discussed in Section 5.6.3. For the minimum rectified DC of 302 V (Section 5.6.2.3), this is  $0.75 \times 302$  or 227 V. This compares favorably to the 370 V DC at maximum AC input as calculated in Section 5.6.2.3.

The peak current from the bucked-down 227 V will not differ much from the 10.3 A calculated in Section 5.6.2.3. Thus assume a total efficiency of 80%, as for the circuit of Figure 5.8. Assume that half the losses are in the bridge and half in the buck regulator of Figure 5.9. Then for a bridge efficiency of 90%, its input power is  $2000/0.9$  or 2222 W. With a preregulated input, the bridge transistors can operate at 90% duty cycle without concern about simultaneous conduction. Input power is then  $0.9I_p V_{dc} = 2222$  W. For  $V_{dc}$  of 227 V as above, this yields  $I_p$  of 10.8 A. Calculating bridge transistor dissipation as in Section 5.6.2.3 for a current fall time  $t_f$  of 0.3  $\mu$ s out of a period  $T$  of 20  $\mu$ s, dissipation per transistor is  $(I_p/2)(V_{dc})(t_f/T) = (10.8/2)227 \times 0.3/20 = 18.4$  W. This is 74 W for the entire bridge as compared to 114 W for the circuit of Figure 5.8 as calculated in Section 5.6.2.3.

### 5.6.4.4 Flux-Imbalance Problem in Bridge Transformer

This problem is still the same as in the topology of Figure 5.8. A volt-second unbalance can occur because of unequal storage times for bipolar bridge transistors or because of unequal “on” voltages for MOSFET transistors. The solution for both the Figure 5.8 and Figure 5.9 topologies is to insert a DC blocking capacitor in series with the transformer primary.



### 5.6.5 Drawbacks in Buck Voltage-Fed Full-Wave Bridge<sup>9,10</sup>

Despite the advantages over the pulse-width-modulated full-wave inverter bridge, the buck voltage-fed full-wave bridge has a number of significant drawbacks.

First, there are the added cost, volume, and power dissipation of the buck transistor  $Q5$  (Figure 5.9) and the cost and volume of the buck  $LC$  filter ( $L1$ ,  $C1$ ). The added cost and volume of these elements is partly compensated by the saving of an inductor at each output. The added dissipations of the buck regulator  $Q5$  and the free-wheeling diode  $D5$  are most often a small percentage of the total losses for a  $\geq 2000$ -W power supply.

Second, there are turn “on” and turn “off” transient losses in the buck transistor, which can be greater than its DC conduction losses. These can be reduced in the transistor by diverting them to passive elements in snubbers. But the losses, cost, and required space of the snubbers is still a drawback. Turn “on”–turn “off” snubbers will be discussed in the later section on the buck current-fed full-wave bridge.

The turn “off” transient losses in the bridge transistors, although less than for the pulse-width-modulated bridge of Figure 5.8, still remain significant. (See the discussion in Section 5.6.4.3.)

Finally, under conditions of unusually long storage time at high temperature and low load or low line, at the turn “on” of one transistor pair, the opposite pair may still be “on.” With the low-source impedance of the buck filter capacitor and the momentary short circuit across the supply bus, this will cause immediate failure of at least one, and possibly all, of the bridge transistors.

### 5.6.6 Buck Current-Fed Full-Wave Bridge Topology—Basic Operation<sup>9,10</sup>

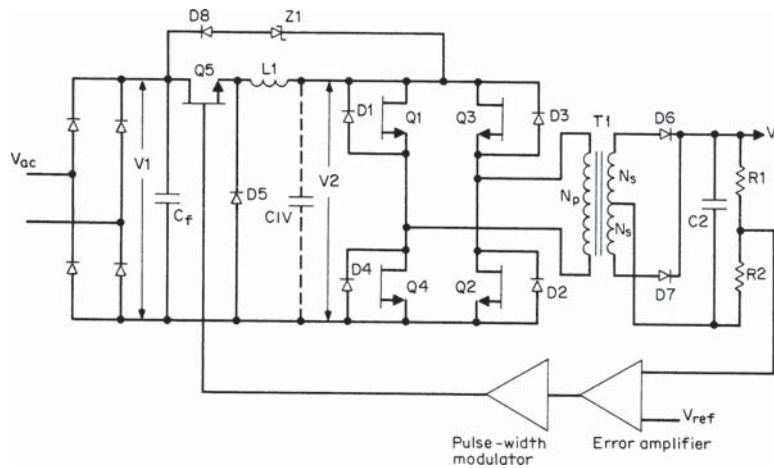
This topology is shown in Figure 5.10.<sup>6</sup> It has no output inductors and is exactly like the buck voltage-fed full-wave bridge of Figure 5.9 with the exception that there is no buck filter capacitor  $C1$ . Instead, there is a virtual capacitor  $C1V$ , which is the sum of all the secondary filter capacitors reflected by the squares of their respective turns ratios into the  $T1$  primary. The filtering by this virtual capacitor  $C1V$  is exactly the same as that of a real capacitor of equal magnitude.

Thus, by replacing all the output inductors of the pulse-width-modulated full-wave bridge of Figure 5.8 with a single primary side inductor as in Figure 5.9, all the advantages described in Section 5.6.2.1 for the Figure 5.9 circuit are also obtained for the circuit of Figure 5.10.

Bridge transistors  $Q1$  to  $Q4$  are not pulse-width-modulated, as they were in Figure 5.8. In this topology, diagonally opposite transistors are



## 194 Switching Power Supply Design



**FIGURE 5.10** Buck current-fed full-wave bridge. The buck filter capacitor  $C_1$  is omitted. There is a virtual capacitor  $C1V$  there—it is the sum of all the output capacitors of the master and slaves reflected into the primary. Diagonally opposite transistors are turned “on” simultaneously. By causing the “off”-turning and “on”-turning pair to overlap in the “on” state for a short time ( $\sim 1\ \mu\text{s}$ ), significant advantages are obtained. During the overlap of the “off”- and “on”-turning pairs, the high impedance looking into  $L_1$  (with  $C_1$  missing) forces all input and output nodes of the bridge to collapse to zero volts. It is the high impedance looking back into  $L_1$  that gives the source driving the bridge the characteristic of a constant current generator.  $Z_1$ ,  $D_8$  constitute an upper clamp to limit  $V_2$  when the previously “on” transistors turn “off.”

simultaneously “on” during alternate half cycles without the normal “off dead time” between the turn “off” of one pair and the turn “on” of the next pair, as was required for the voltage-fed circuit of Figure 5.9. Each pair in Figure 5.10 is kept “on” deliberately for slightly more than a half period, either by depending on the storage times of slow bipolar transistors or by delaying the turn “off” time by  $\sim 1\ \mu\text{s}$  or so when using faster bipolar or MOSFET devices. Output voltage regulation is achieved by pulse-width-modulating the “on” time of the buck transistor  $Q_5$  as was done for the buck voltage-fed circuit of Figure 5.9.

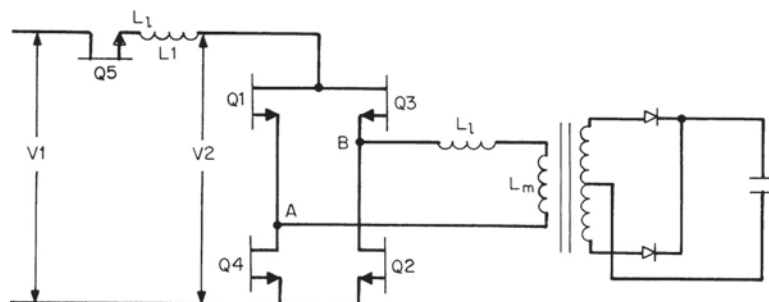
Significant advantages accrue from the physical removal of buck filter capacitor  $C_1$  of Figure 5.9 and the deliberate overlapping “on” times of alternate transistor pairs. These advantages are described as follows.

### 5.6.6.1 Alleviation of Turn “On”–Turn “Off” Transient Problems in Buck Current-Fed Bridge<sup>9,10</sup>

For the pulse-width-modulated full-wave bridge of Figure 5.8, Section 5.6.2.2 described excessive current, power dissipation stresses in the bridge transistors, and voltage stresses in the output rectifier diodes at the instant of turn “on.” Such stresses do not occur in the current-fed circuit of Figure 5.10 because of the overlapping “on” times of alternate transistor pairs and the high impedance seen looking back into  $L_1$  with no filter capacitor physically present at that node.

This can be seen from Figures 5.11 and 5.12. Consider in these figures that  $Q_3, Q_4$  had been “on” and  $Q_1, Q_2$  commence turning “on” at  $T_1$ . Transistors  $Q_3, Q_4$  remain “on” until  $T_2$  (Figure 5.12), resulting in an overlap time of  $T_2 - T_1$ . At  $T_1$ , as  $Q_1, Q_2$  come “on,” a dead short circuit appears at the output of  $L_1$ , and since the impedance looking into  $L_1$  is high, the voltage  $V_2$  collapses to zero (Figure 5.12c).  $L_1$  is a large inductor and current in it must remain constant at its initial value  $I_L$ . Thus as current in  $Q_1, Q_2$  rises from zero toward  $I_L$  (Figure 5.12f and 5.12g), current in  $Q_3, Q_4$  falls from  $I_L$  toward zero (Figure 5.12d and 5.12e).

Note, the rising current in  $Q_1, Q_2$  occurs with zero voltage at  $V_2$ , so there is also zero voltage between nodes  $A$  and  $B$  in Figure 5.11. Hence, there is no voltage across  $Q_1, Q_2$  as their current rises, and there is no dissipation in them. At some later time  $T_3$ , currents in  $Q_1, Q_2$  have risen to  $I_L/2$  and currents in  $Q_3, Q_4$  have fallen from  $I_L$  to  $I_L/2$ , thus summing to the constant current  $I_L$  from inductor  $L_1$ .



**FIGURE 5.11** During the overlap, when all four transistors are “on,” the voltage  $V_2$  and that across nodes  $A, B$  collapse to zero. Energy stored in leakage inductance  $L_1$  is fed to the load via the transformer instead of being dissipated in a snubber resistor or being returned to the input bus as in conventional circuits. Hence, there is no turn “on” transient dissipation in the bridge transistors or overvoltage stress in output rectifiers.

## 196 Switching Power Supply Design

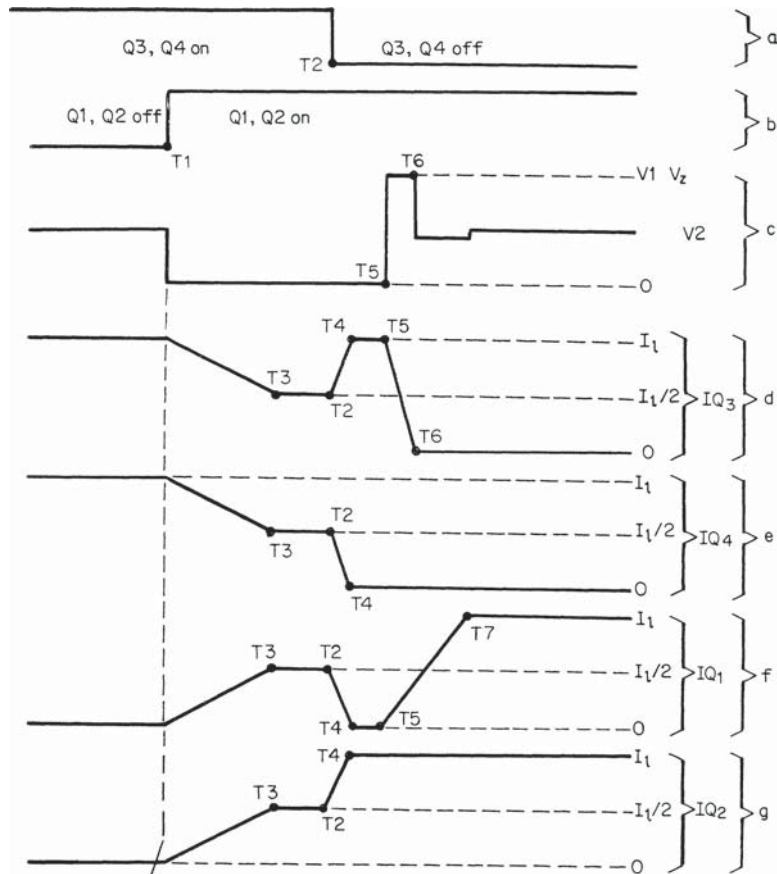
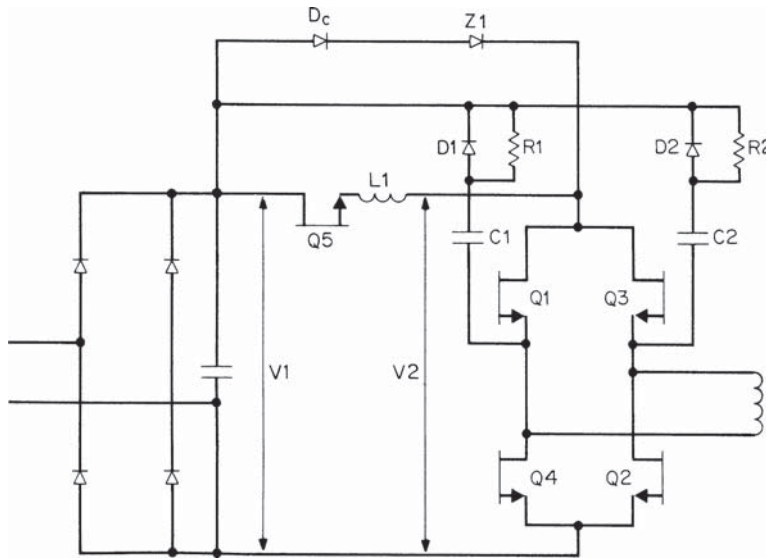


FIGURE 5.12 Current waveforms in bridge transistors and voltages at bridge input during the overlapping “on” times of all four bridge transistors in buck current-fed topology.

Assume, as a worst-case scenario, that  $Q3$  is slower than  $Q4$ , and  $Q4$  turns “off” first. Note that at  $T_2$ , when  $Q3$  and  $Q4$  are commanded “off,” the voltage  $V_2$  is zero, so  $Q4$  turns “off” with zero voltage across it and little turn “off” dissipation. As  $I_{Q4}$  falls from  $I_L/2$  toward zero ( $T_2$  to  $T_4$ ),  $I_{Q2}$  rises from  $I_L/2$  toward  $I_L$  to maintain the constant  $I_L$  demanded by  $L1$ . As  $I_{Q2}$  rises from  $I_L/2$  toward  $I_L$ ,  $I_{Q3}$  rises from  $I_L/2$  to  $I_L$  to supply  $I_{Q2}$ . Again, since  $L1$  demands a constant current  $I_L$ , as  $I_{Q3}$  rises toward  $I_L$ ,  $I_{Q1}$  falls from  $I_L/2$  to zero at  $T_4$ .

During the time  $T_1$  to  $T_4$ , while  $V_2$  is zero volts, the voltage across the transformer primary ( $A$  to  $B$  in Figure 5.11) will also fall. Current



**FIGURE 5.13** The buck current-fed bridge. In this circuit only two turn “off” snubbers ( $R1, C1, D1$  and  $R2, C2, D2$ ) are required. An upper voltage clamp ( $Z1, Dc$ ) is required to limit  $V2$  when the last of the “off”-turning transistors turns “off.”

had been stored in the transformer leakage inductance  $L_L$  while  $Q3, Q4$  were “on.” As voltage  $A$  to  $B$  collapses, the voltage across the primary leakage inductance reverses to keep the current constant. Thus the leakage inductance acts like a generator and delivers this stored energy through the transformer to the secondary load instead of returning it to the input supply bus or to dissipative snubbers as in conventional circuits.

At a later time  $T_5$ , the slower transistor  $Q3$  starts turning “off.” As current in it falls from  $I_L$  to zero (Figure 5.12d), current  $I_{Q1}$  tries to rise from zero to  $I_L$  to maintain the constant current  $I_L$  demanded by  $L1$ . But  $I_{Q1}$  rise time is limited by the transformer leakage inductance (Figure 5.12f). Since  $I_{Q3}$  fall time is generally greater than  $I_{Q1}$  rise time, voltage  $V_2$  will overshoot its quiescent value and must be clamped to avoid overstressing  $Q3$ , as its emitter is now clamped to ground by the conducting  $Q2$ . The clamping is done by a zener diode  $Z1$ , as shown in Figures 5.10 and 5.13.

Voltage overshoot of  $V_2$  during the slower transistor ( $Q3$ ) turn “off” time results in somewhat more dissipation in it than in the circuit of the conventional pulse-width-modulated bridge (Figure 5.8). This dissipation is  $(V_1 + V_z)(I_L/2)(T_6 - T_5)/T$  for Figure 5.10, but only

## 198 Switching Power Supply Design

$V_1(I_L/2)(T_6 - T_5)/T$  for Figure 5.8. In Figure 5.8, there are four transistors that have relatively high turn “off” dissipation. In Figures 5.10 and 5.13, only the two transistors with slow turn “off” time have high dissipation. As discussed above, the faster transistor suffers no dissipation at turn “off” as it turns “off” at zero voltage; and at turn “on,” all transistors have negligible dissipation, because the transformer leakage inductance is in series with them, so they turn “on” at zero voltage.

The increased dissipation of the two transistors at turn “off” can be diverted from the transistors to resistors by adding the snubbing networks  $R1, C1, D1$  and  $R2, C2, D2$  of Figure 5.13. Design of such turn “off” snubbing circuits will be discussed in the later chapter on snubbers.

### 5.6.6.2 Absence of Simultaneous Conduction Problem in the Buck Current-Fed Bridge

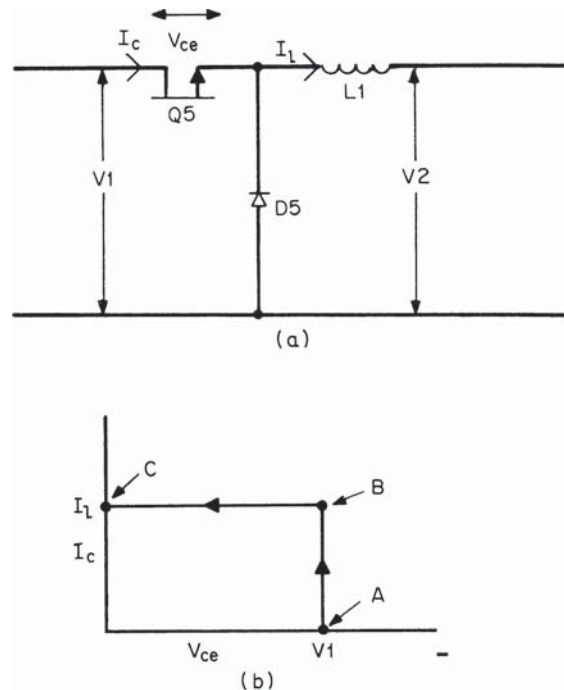
In the buck voltage-fed bridge of Figure 5.9, care must be taken to avoid simultaneous conduction in transistors positioned vertically above one another ( $Q1, Q4$  or  $Q3, Q2$ ). Such simultaneous conduction comprises a short circuit across  $C1$ . Since  $C1$  has a low impedance, it can supply large currents without its output ( $V_2$ ) dropping very much. Thus the bridge transistors could be subjected to simultaneous high voltage and high current, and one or more would immediately fail.

Even if a dead time between the turn “off” of one transistor pair and the turn “on” of the other is designed in to avoid simultaneous conduction, it still may occur under various odd circumstances, such as high temperature and/or high load conditions when transistor storage time may be much lower than data sheets indicate or low input voltage (in the absence of maximum “on” time clamp or undervoltage lockout) as the feedback loop increases “on” time to maintain constant output voltage.

But in the buck current-fed bridge, simultaneous conduction is actually essential to its operation and the inductor limits the current, hence it provides the advantages discussed above. Further, in the buck current-fed bridge, since the “on” time is slightly more than a half period for each transistor pair, the peak current is less than in the buck voltage-fed bridge, whose maximum “on” time is usually set at 90% of a half period to avoid simultaneous conduction.

### 5.6.6.3 Turn “On” Problems in Buck Transistor of Buck Current- or Buck Voltage-Fed Bridge<sup>10</sup>

The buck transistor in either the voltage- or current-fed bridge suffers from a large spike of power dissipation at the instant both of turn “on” and turn “off,” as can be seen in Figure 5.14.



**FIGURE 5.14** (a) The buck transistor in the buck current- or voltage-fed topology has a very unfavorable voltage-current locus at the instant of turn "on." It operates throughout its current rise time at the full input voltage  $V_1$  until the forward current in free-wheeling diode  $D_5$  has been canceled. This generates a large spike of dissipation at turn "on." (b)  $I_c$  vs.  $V_{ce}$  locus during turn "on" of buck transistor  $Q_5$ . Voltage  $V_{ce}$  remains constant at  $V_1$  until the current in  $Q_5$  has risen to  $I_L$  (A to B) and canceled the forward current  $I_L$  in free-wheeling diode  $D_5$ . Then, if capacitance at the  $Q_5$  emitter is low and  $D_5$  has a fast recovery time, it moves very rapidly to its "on" voltage of about 1 V (B to C).

**After Pressman** Because  $L_1$  forces a constant current to flow in  $Q_5$  as it turns "off,"  $Q_5$  is subject to both an increasing voltage and a constant current until the emitter voltage drops below zero, when  $D_5$  conducts and the  $L_1$  current commutates from  $Q_5$  to  $D_5$ . The peak power occurs at half voltage, when  $P_p = V_1/2 \times I_L$ . Faster switching devices will reduce the average power loss, but cannot reduce the peak power unless an alternative path is provided for the  $L_1$  current during the turn "off" edge of  $Q_5$ . ~K.B.

Consider first the instantaneous voltage and current of  $Q_5$  during the turn "on" interval. The locus of rising current and falling voltage

## 200 Switching Power Supply Design

during that interval is shown in Figure 5.14*b*. Just prior to  $Q5$  turning “on,” free-wheeling diode  $D5$  is conducting and supplying inductor current  $I_L$ . As  $Q5$  commences turning “on,” its collector is at  $V_1$ , its emitter is at one diode ( $D5$ ) drop below common. The emitter does not move up from common until the current in  $Q5$  has risen from zero to  $I_L$  and canceled the  $D5$  forward current.

Thus, during the current rise time to  $t_r$ , the  $I_c - V_{ce}$  locus is from points  $A$  to  $B$ . During  $t_r$ , the average current supplied by  $Q5$  is  $I_L/2$  and the voltage across it is  $V_1$ . Once current in  $Q5$  has risen to  $I_L$ , assuming negligible capacitance at the  $Q5$  emitter node and fast recovery time in  $D5$ , the voltage across  $Q5$  rapidly drops to zero along the path  $B$  to  $C$ . If there is one turn “on” of duration  $t_r$  in a period  $T$ , the dissipation in  $Q5$ , averaged over  $T$ , is

$$PD_{\text{turnon}} = V_1 \frac{I_L t_r}{2T} \quad (5.10)$$

It is of interest to calculate this dissipation for a 2000-W buck current-fed bridge operating from the rectified 220-V AC line. Nominal rectified DC voltage ( $V_1$ ) is about 300 V, minimum is 270 V, and maximum is 330 V. Assume that the bucked-down DC voltage  $V_2$  is 25% below the minimum  $V_1$  or about 200 V.

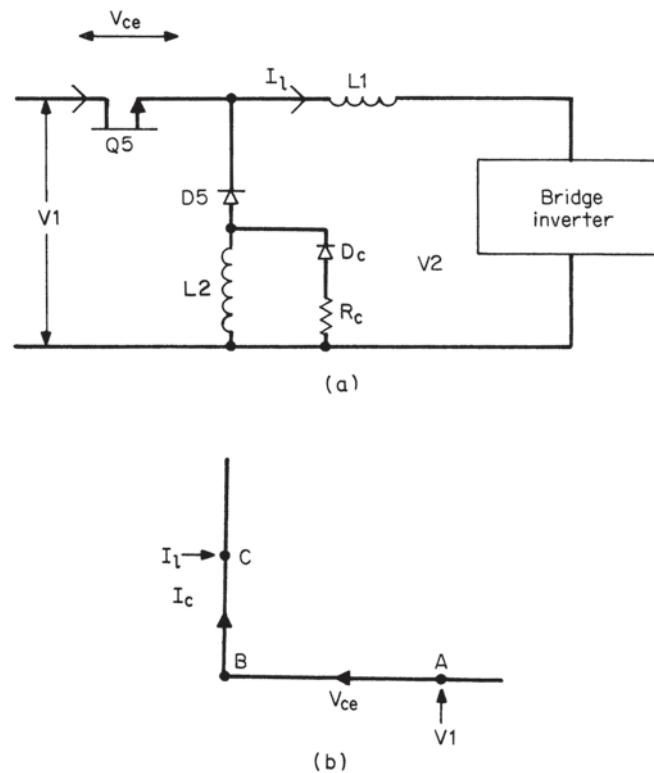
Further, assume the bridge inverter operates at 80% efficiency, giving an input power of 2500 W. This power comes from a  $V_1$  of 200 V, and hence the average current in  $L1$  is 12.5 A. Assume that  $L1$  is large enough so that the ripple current in  $I_L$  can be neglected.

Then, for an assumed 0.3- $\mu$ s current rise time (easily achieved with modern bipolar transistors) and a  $Q5$  switching frequency of 50 kHz, turn “on” dissipation at maximum AC input voltage is (from Eq. 5.10)

$$PD = 330 \left( \frac{12.5}{2} \right) \left( \frac{0.3}{20} \right) = 31 \text{ W}$$

Note in this calculation that the effect of poor recovery time in  $D5$  has been neglected. This has been discussed in Section 5.6.2.2 in connection with the poor recovery time of output rectifiers of the bridge inverter. This problem can be far more serious for the free-wheeling diode of the buck regulator, for  $D5$  must have a much higher voltage rating—at least 400 V for the maximum  $V_1$  of 330 V—and high-voltage diodes have poorer recovery times than lower-voltage ones. Thus the  $Q5$  current can considerably overshoot the peak of 12.5 A that  $D5$  had been carrying. Further, the oscillatory ring after the recovery time, discussed in Section 5.6.2.2, can cause a serious voltage overstress in free-wheeling diode  $D5$ .

Turn “on” dissipation in  $Q5$  and voltage overstress of  $D5$  can be eliminated with the turn “on” snubber of Figure 5.15.



**FIGURE 5.15** (a) Turn “on” snubber— $L2$ ,  $D_c$ ,  $R_c$ —eliminates turn “on” dissipation in  $Q5$ , but at the price of an equal dissipation in  $R_c$ . When  $Q5$  commences turning “on,”  $L2$  drives the  $Q5$  emitter voltage up to within 1 V of its collector. As  $Q5$  current rises toward  $I_L$ , the current in  $L2$ , which has been stored in it by  $L1$  during the  $Q5$  “off” time, decreases to zero. Thus the voltage across  $Q5$  during its turn “on” time is about 1 V rather than  $V1$ . During the next  $Q5$  “off” time,  $L2$  must be charged to a current  $I_L$  without permitting too large a drop across it. Resistor  $R_c$  limits the voltage across  $L2$  during its charging time. (b)  $Q5$ ’s locus of falling voltage (A to B) and rising current (B to C) during turn “on,” with the snubber of Figure 5.15a.

#### 5.6.6.4 Buck Transistor Turn “On” Snubber—Basic Operation

The turn “on” snubber of Figure 5.15a does not reduce circuit dissipation. Power is diverted from the vulnerable semiconductor  $Q5$ , where it is a potential failure hazard, to the passive resistor  $R_s$ , which can far more easily survive the heat. It works as follows. An inductor  $L2$  is added in series with the free-wheeling diode  $D5$ . While  $Q5$  is “off,” the inductor load current  $I_L$  flows out of the bottom of the bridge



## 202 Switching Power Supply Design

transistors, up through the bottom end of  $L2$ , through free-wheeling diode  $D5$ , and back into the front end of  $L1$ . This causes the top end of  $L2$  to be slightly more negative than its bottom end.

As  $Q5$  commences turning “on,” it starts delivering current into the cathode of  $D5$  to cancel its forward current. This current flows down into  $L2$ , opposing the load current it is carrying. Since the current in an inductor ( $L2$ ) cannot change instantaneously, the voltage polarity across it reverses instantaneously to maintain constant current.

The voltage at the top end of  $L2$  rises, pushing the free-wheeling diode cathode up with it until it meets the “on”-turning  $Q5$  emitter voltage. The  $Q5$  emitter is forced up to within  $V_{ce(sat)}$  of its collector, and now  $Q5$  continues increasing its current, but at a  $V_{ce}$  voltage of about 1 V rather than the  $V_1$  voltage of 370 V it had to sustain in the absence of  $L2$ .

When the  $Q5$  current has risen to  $I_L$  (in a time  $t_r$ ), the forward current in  $D5$  has been canceled and  $Q5$  continues to supply the load current  $I_L$  demanded by  $L1$ . Since the voltage across  $Q5$  during the rise time  $t_r$  is only 1 V, its dissipation is negligible. Further, because of the high impedance of  $L2$  in series with the  $D5$  anode, there is negligible recovery time current in  $D5$ . The current-voltage locus of  $Q5$  during the turn “on” time is shown in Figure 5.15*b*.

### 5.6.6.5 Selection of Buck Turn “On” Snubber Components

For the preceding sequence of events to proceed as described, the current in  $L2$  must be equal to the load current  $I_L$  at the start of  $Q5$  turn “on” and must have decayed back down to zero in the time  $t_r$  that current from  $Q5$  has risen to  $I_L$ . Since the voltage across  $L2$  during  $t_r$  is clamped to  $V_1$ , the magnitude of  $L2$  is calculated from

$$L2 = \frac{V_1 t_r}{I_L} \quad (5.11)$$

For the above example,  $V_1$  was a maximum of 330 V,  $t_r$  was 0.3  $\mu$ s, and  $I_L$  was 12.5 A. From Eq. 5.11, this yields  $L2 = 330 \times 0.3/12.5 = 7.9 \mu$ H.

The purpose of  $R_c$ ,  $D_c$  in Figure 5.15*a* is to ensure that at the start of  $Q5$  turn “on,” current in  $L2$  truly is equal to  $I_L$  and that it has reached that value without overstressing  $Q5$ .

Consider, for the moment, that  $R_c$ ,  $D_c$  were not present. As  $Q5$  turned “off,” since current in  $L1$  cannot change instantaneously, the input end of  $L1$  goes immediately negative to keep current constant. If  $L2$  were not present,  $D5$  would clamp the front end of  $L1$  (and hence the  $Q5$  emitter) at common, and permit a voltage of only  $V_1$  across  $Q5$ . But with  $L2$  present, the impedance looking out of the  $D5$  anode is the high instantaneous impedance of  $L2$ . As  $Q5$  turned “off,”  $I_L$  would be drawn through  $L2$ , pulling its top end far negative. This would put

a large negative voltage at the  $Q_5$  emitter, and with its collector at  $V_1$  (370 V in this case), it would immediately fail.

Thus  $R_c$  and  $D_c$  are shunted around  $L_2$  to provide a path for  $I_L$  at the instant  $Q_5$  turns “off,” and  $R_c$  is selected low enough so that the voltage drop across it at a current  $I_L$  plus  $V_1$  is a voltage stress that  $Q_5$  can safely take. Thus

$$V_{Q5(\max)} = V_1 + R_c I_L \quad (5.12)$$

In the preceding example,  $V_{1(\max)}$  was 330 V. Assume that  $Q_5$  had a  $V_{ce0}$  rating of 450 V. With a t1- to t5-V reverse bias at its base at the instant of turn “off,” it could safely sustain the  $V_{cev}$  rating of 650 V. Then to provide a margin of safety, select  $R_c$  so that  $V_{Q5(\max)}$  is only 450 V. Then from Eq. 5.12,  $450 = 330 + R_c \times 12.5$  or  $R_c = 9.6\Omega$ .

#### 5.6.6.6 Dissipation in Buck Transistor Snubber Resistor

Examination of Figure 5.15a shows that essentially the constant current  $I_L$  is charging the parallel combination of  $R_c$  and  $L_2$ . The Thevenin equivalent of this is a voltage source of magnitude  $I_L R_c$  charging a series combination of  $R_c$  and  $L_2$ . It is well known that in charging a series inductor  $L$  to a current  $I_p$  or energy  $\frac{1}{2}LI_p^2$ , an equal amount of energy is delivered to the charging resistor. If  $L$  is charged to  $I_p$  once per period  $T$ , the dissipation in the resistor is  $\frac{1}{2}LI_p^2/T$ .

In the preceding example where  $T = 2\mu\text{s}$ ,  $L = 7.9\mu\text{H}$ , and  $I_p = 12.5\text{ A}$

$$\begin{aligned} PD_{\text{snubber resistor}} &= \frac{(1/2)(7.9)(12.5)^2}{20} \\ &= 31\text{ W} \end{aligned}$$

Thus, as mentioned above, this snubber has not reduced circuit dissipation; it has only diverted it from the transistor  $Q_5$  to the snubbing resistor.

#### 5.6.6.7 Snubbing Inductor Charging Time

The snubbing inductor must be fully charged to  $I_L$  during the “off” time of the buck transistor. The charging time constant is  $L/R$ , which in the above example is  $7.9/6.4 = 1.23\mu\text{s}$ . The inductor is 95% fully charged in three time constants or  $3.7\mu\text{s}$ .

In the preceding example, switching period  $T$  was  $20\mu\text{s}$ . To buck down the input of 330 V to the preregulated 200 V, “on” time is  $T_{\text{on}} = 20(200/330) = 12\mu\text{s}$ . This leaves a  $Q_5$  “off” time of  $8\mu\text{s}$ , which is sufficient, as the snubbing inductor is 95% fully charged in  $3.7\mu\text{s}$ .

## 204 Switching Power Supply Design

5.6.6.8 Lossless Turn "On" Snubber for Buck Transistor<sup>10,21,22</sup>

Losses in the snubbing resistor of Figure 5.15a can be avoided with the circuit of Figure 5.16. Here, a small transformer  $T2$  is added. Its primary turns  $N_p$  and gap are selected so that at a current  $I_L$ , its inductance is the same as  $L2$  of Figure 5.15a. The polarities at the primary and secondary are as shown by the dots.

When  $Q5$  turns "off," the front end of  $L1$  goes negative to keep  $I_L$  constant.  $I_L$  flows through  $D5$  and  $N_p$ , producing a negative voltage  $V_n$  at the dot end of  $N_p$  and voltage stress across  $Q5$  of  $V_1 + V_n$ . Voltage  $V_n$  is chosen so that  $V_1 + V_n$  is a voltage that  $Q5$  can safely sustain. To maintain the voltage across  $N_p$  at  $V_n$  when  $Q5$  has turned "off," the turns ratio  $N_s/N_p$  is selected equal to  $V_1/V_n$ . When  $Q5$  turns "off," as the dot end of  $N_p$  goes down to  $V_n$ , the no-dot end of  $N_s$  goes positive and is clamped to  $V_1$ , holding the voltage across  $N_p$  to  $V_n$ .

Prior to  $Q5$  turn "on,"  $L1$  current flows through  $N_p$ ,  $D5$ . As  $Q5$  commences turning "on," its emitter looks into the high impedance of  $N_p$  and immediately rises to within one volt of its collector. Thus, current in  $Q5$  rises with only one volt across it, and its dissipation is negligible. All the energy stored in  $N_p$  when  $Q5$  was "off," is returned via  $L1$  to the load with no dissipation.  $Q5$  turn "off" dissipation can be minimized with a turn "off" snubber (Chapter 11).

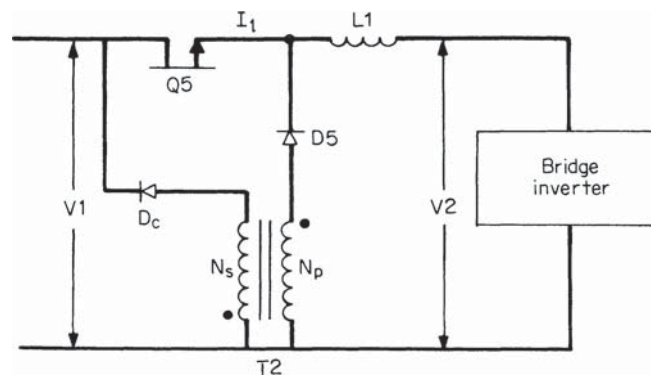


FIGURE 5.16 Non-dissipative turn "on" snubber. When  $Q5$  turns "off,"  $L1$  stores a current  $I_L$  in  $N_p$  of  $T1$ . The negative voltage at the dot end of  $N_p$  during this charging time is fixed by the turns ratio  $N_s/N_p$ . If the top end of  $N_p$  is to be permitted to go to only  $V_n$  negative when  $Q5$  turns "off," the voltage stress on  $Q5$  is  $V_1 + V_n$ . When the dot end of  $N_p$  has gone negative to  $V_n$ , the no-dot end of  $N_s$  has been driven up to  $V_1$ ,  $D_c$  clamps to  $V_1$ , clamping the voltage across  $N_p$  to the preselected  $V_n$ . Thus  $N_s/N_p$  is chosen as  $V_1/V_n$ . The charging of  $N_p$  is not limited by a resistor as in Figure 5.14, so there is no snubber dissipation.

### 5.6.6.9 Design Decisions In Buck Current-Fed Bridge

The first decision to be made on the buck current-fed bridge is when to use it. It is primarily a high-output-power, high-output-voltage topology.

In terms of cost, efficiency, and required space, it is a good choice for output powers in the range of 1 to 10 or possibly 20 kW. For high-output voltages—above about 200 V—and above about 5 A output current—the absence of output inductors makes it a good choice. For output powers above 1 kW, the added dissipation, volume, and cost of the buck transistor is not a significant increase above what is required in a competing topology such as a pulse-width-modulated full-wave bridge.

It is an especially good choice for a multi-output supply consisting of one or more high-output voltages (5000 to 30,000 V). In such applications, the absence of output inductors permits the use of capacitor-diode voltage multiplier chains.<sup>8,13</sup> Also, the absence of output inductors in the associated lower-output voltages partly compensates for the cost and volume of the buck transistor and its output inductor.

The next design decision is the selection of the bucked-down voltage ( $V_2$  of Figure 5.10). This is chosen at about 25% below the lowest ripple trough of  $V_1$  (Figure 5.10) at the lowest specified AC input. Inductor  $L_1$  is chosen for continuous operation at the calculated minimum inductor current  $I_L$  corresponding to the minimum total output power at the preselected value of  $V_2$ . It is chosen as in Section 1.3.6 for a conventional buck regulator.

The output capacitors are not chosen to provide storage or reduce ripple directly at the output, because the overlapping conduction of bridge transistors minimizes this requirement. Rather they are chosen so that when reflected into the primary, the equivalent series resistance  $R_{esr}$  of all reflected capacitors is sufficiently low as to minimize ripple at  $V_2$ . Recall from Section 1.3.7, in calculating the magnitude of the output capacitor, it was pointed out that output ripple in a buck regulator  $V_{br}$  is given by

$$V_{br} = \Delta I R_{esr}$$

in which  $\Delta I$  is the peak-to-peak ripple current in the buck inductor and is usually set at twice the minimum DC current in it so that the inductor is on the threshold of discontinuous operation at its minimum DC current. Minimum DC current in this case is the current at minimum specified output power at the preselected value of  $V_2$ . Thus with  $R_{esr}$  selected so as to yield the desired ripple at  $V_2$ , ripple at each secondary is

$$V_{sr} = V_{br} \frac{N_s}{N_p}$$

## 206 Switching Power Supply Design

There is an interesting contrast in comparing a current- to a voltage-fed bridge at the same bucked-down voltage ( $V_2$  of Figures 5.9 and 5.10).

For the voltage-fed bridge, a maximum “on” time of 80% of a half period must be established to ensure that there is no simultaneous conduction in the two transistors positioned vertically one above another. With the low impedance looking back into the buck regulator of the voltage-fed circuit, such simultaneous conduction would subject the bridge transistors to high voltage and high current and destroy one or more of them.

In the current-fed circuit, such slightly overlapping simultaneous conduction is essential to its operation and “on” time of alternate transistor pairs is slightly more than a full half period at any DC input voltage. In addition, since the “on” time of a voltage-fed bridge (Figure 5.9) is only 80% of a half period, its peak current must be 20% greater than that of the current-fed bridge at the same output power.

It should also be noted that the number of primary turns as calculated from Faraday’s law (Eq. 2.7) must be 20% greater in the current-fed bridge, since the “on” time is 20% greater for a flux change equal to that in a voltage-fed bridge at the same  $V_2$ .

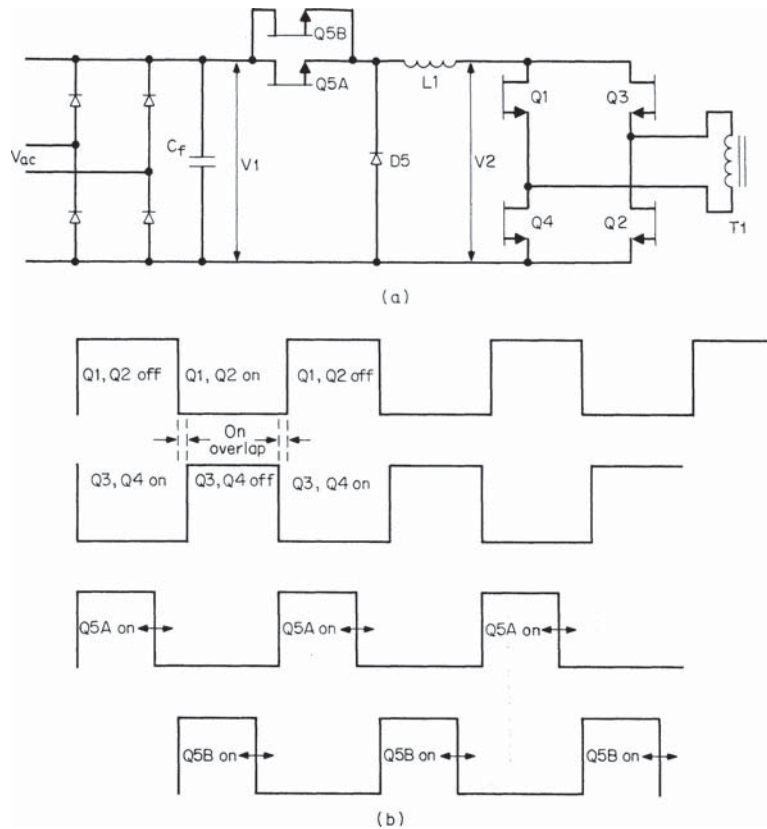
### 5.6.6.10 Operating Frequencies—Buck and Bridge Transistors

The buck transistor is usually synchronized to and operates at twice the square-wave switching frequency of the bridge transistors. Recall that it alone is pulse-width-modulated, and that the bridge devices are operated at a 50-percent duty cycle with a slightly overlapping “on” time.

Frequently, however, the scheme of Figure 5.17a with two buck transistors ( $Q5A$  and  $Q5B$ ) is used to reduce dissipation. They are synchronized to the bridge transistor frequency and are turned “on” and pulse-width-modulated on alternate half cycles of the bridge square-wave frequency. Thus the DC and switching losses are shared between two transistors with a resulting increase in reliability.

### 5.6.6.11 Buck Current-Fed Push-Pull Topology

The buck current-fed circuit can also be used to drive a push-pull circuit as in Figure 5.18 with the consequent saving of two transistors over the buck current-fed bridge. Most of the advantages of the buck current-fed bridge are realized and the only disadvantage is that the push-pull circuit power transistors have greater voltage stress. This voltage stress is twice  $V_2$ , rather than  $V_2$  as in the bridge circuit. But  $V_2$  is the pre-regulated and bucked-down input voltage—usually only 75% of the minimum  $V_1$  input. This is usually about the same as the maximum DC input of a competing topology—like the pulse-width-modulated full-wave bridge (Figure 5.8).

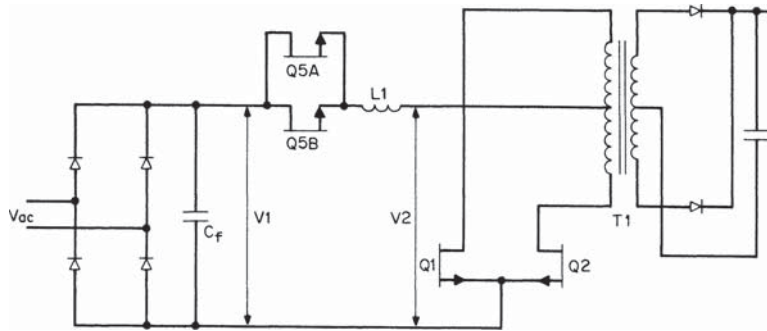


**FIGURE 5.17** (a) Buck transistor  $Q5$  can be a single transistor operating at twice the frequency of the bridge transistors and synchronized to them, or more usually, it is two synchronized transistors that are both pulse-width-modulated and are "on" during alternate half periods of the bridge transistors. (b) To reduce dissipation in the buck transistor, it is usually implemented as two transistors, each synchronized to the bridge transistors and operated at the same square-wave frequency as the bridge devices. Transistors  $Q5A$ ,  $Q5B$  are pulse-width-modulated. Bridge transistors are not and are operated with a small "on" overlap time.

However, the major advantages of the current-fed technique—no output inductors and no possibility of flux imbalance—still exist.

The topology can be used to greatest advantage in supplies of 2 to 5 kW, especially if there are multiple outputs or at least one high-voltage output.

## 208 Switching Power Supply Design



**FIGURE 5.18** The current-fed topology can also be implemented as a buck push-pull circuit. As in the buck current-fed bridge, the capacitor after the buck inductor  $L1$  is omitted, and  $Q1$ ,  $Q2$  are operated with a deliberately overlapping “on” time. Only buck transistors  $Q5A$ ,  $Q5B$  are pulse-width-modulated. Output inductors are not used. All the advantages of the buck current-fed bridge are retained. Although “off”-voltage stress is twice  $V2$  (plus a leakage spike) instead of  $V2$  as in the bridge, it is still significantly less than twice  $V1$  because  $V2$  is bucked down to about 75% of the minimum value of  $V1$ . This circuit is used at lower power levels than the buck current-fed bridge and offers the savings of two transistors.

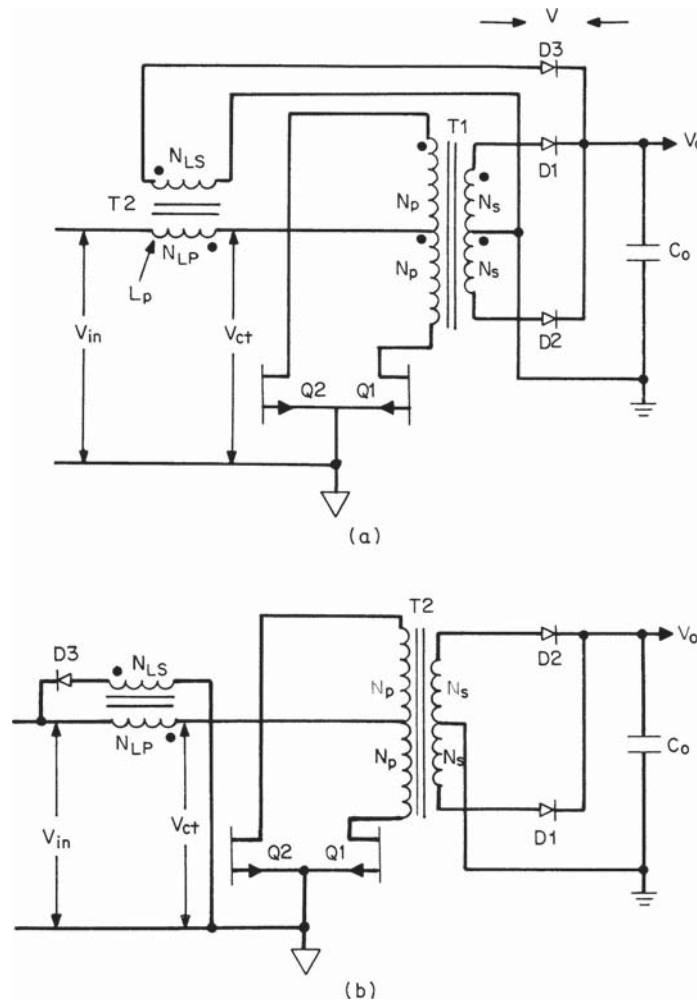
### 5.6.7 Flyback Current-Fed Push-Pull Topology (Weinberg Circuit <sup>23</sup>)

This topology<sup>1,23</sup> is shown in Figure 5.19. Effectively it has a flyback transformer in series with a push-pull inverter. It has many of the valuable attributes of the buck current-fed push-pull topology (Figure 5.18), and since it requires no pulse-width-modulated input transistor ( $Q5$ ), it has lower dissipation, cost, and volume, and greater reliability.

It might be puzzling at first glance to see how the output voltage is regulated against line and load changes, since there is no  $LC$  voltage-averaging filter at the output. The diode-capacitor at the output is a peak, rather than an averaging, circuit. The answer is that the averaging or regulating is done at the push-pull center tap to keep  $V_{ct}$  relatively constant. The output voltage (or voltages) is (are) kept constant by pulse-width-modulating the  $Q1$ ,  $Q2$  “on” time. Output voltage is simply  $(N_s/N_p)V_{ct}$  and a feedback loop sensing  $V_o$  controls the  $Q1$ ,  $Q2$  “on” times to keep  $V_{ct}$  at the correct value to maintain  $V_o$  constant. The relation between the  $Q1$ ,  $Q2$  “on” times and output voltage is shown below.

The circuit retains the major advantage of the current-fed technique—a single-input inductor but no output inductors, which makes it a good choice for a multi-output supply with one or more





**FIGURE 5.19** (a) Flyback current-fed push-pull topology (Weinberg circuit<sup>23</sup>). This is essentially a flyback transformer in series with a pulse-width-modulated push-pull inverter. It is used primarily as a multi-output supply with one or more high-voltage outputs, as it requires no output inductors and only the one input flyback transformer  $T2$ . The high impedance seen looking back into the primary of  $T2$  makes it a "current-fed" topology, with all the advantages shown in Figure 5.18. Here, the  $T2$  secondary is shown clamped to  $V_o$ . Transistors  $Q1$ ,  $Q2$  may be operated either with a "dead time" between "on" times or with overlapping "on" times. Its advantage over Figure 5.18 is that it requires no additional input switching transistors. The usual output power level is 1 to 2 kW. (b) Shows the same circuit as Figure 5.19a, but with the flyback secondary clamped to  $V_{in}$ . This results in less input current ripple but more output voltage ripple.



## 210 Switching Power Supply Design

high-voltage outputs. Further, because of the high-source impedance of the flyback transformer primary  $L_1$ , the usual flux-imbalance problem of voltage-fed push-pulls does not result in transformer saturation and consequent transistor failure. Its major usage is at the 1- to 2-kW power level.

Two circuit configurations of the flyback current-fed push-pull topology are shown in Figure 5.19a and 5.19b. Figure 5.19a shows the flyback secondary returned to the output voltage through diode  $D_3$ ; in Figure 5.19b, the diode is returned to the input voltage. When the diode is returned to  $V_o$ , output ripple voltage is minimized; when it is returned to  $V_{in}$ , input ripple current is minimized. Consider first the configuration of Figure 5.19a, where the diode is returned to the output.

The configuration of Figure 5.19a can operate in two significantly different modes. In the first mode,  $Q_1$  and  $Q_2$  are never permitted to have overlapping “on” times at any DC input voltage. In the second mode,  $Q_1$  and  $Q_2$  may have overlapping “on” times throughout the entire range of specified DC input voltage. The circuit can also be set up to shift between the two modes under control of the feedback loop as the input voltage varies.

It will be shown below that in the non-overlapping mode, power is delivered to the secondaries at a center tap voltage  $V_{ct}$  lower than the DC input voltage (buck-like operation) and in the overlapping mode, power is delivered to the secondaries at a center tap voltage  $V_{ct}$  higher than the DC input voltage (boost-like operation). Since  $V_{ct}$  is relatively low in the non-overlapping mode,  $Q_1$ ,  $Q_2$  currents are relatively high for a given output power. But with the lower  $V_{ct}$  voltage, “off”-voltage stress in  $Q_1$ ,  $Q_2$  is relatively low. In the overlapping mode, since  $V_{ct}$  is higher than  $V_{in}$ ,  $Q_1$ ,  $Q_2$  currents are lower for a given output power but “off”-voltage stress in  $Q_1$ ,  $Q_2$  is higher than that for the non-overlapping mode.

The circuit is usually designed not to remain in one mode throughout the full range of input voltages. Rather, it is designed to operate in the overlapping mode with an “on” duty cycle  $T_{on}/T$  greater than 0.5, and in the non-overlapping mode with  $T_{on}/T$  less than 0.5 as the DC input voltage shifts from its minimum to its maximum specified values. This permits proper operation throughout a larger range of DC input voltages than if operation remained within one mode throughout the entire range of DC input voltage.

### 5.6.7.1 Absence of Flux-Imbalance Problem in Flyback Current-Fed Push-Pull Topology

Flux imbalance is not a serious problem in this topology because of the high-impedance current-fed source that feeds the push-pull transformer center tap.

The current-fed nature of the circuit arises from the flyback transformer, which is in series with the push-pull center tap. The high impedance looking back from the push-pull center tap is the magnetizing inductance of the flyback primary.

In a conventional voltage-fed push-pull inverter, unequal volt-second products across the two half primaries cause the flux-imbalance problem (Section 2.2.5). The transformer core moves off center of its hysteresis loop and toward saturation. Because of the low impedance of a voltage source, current to the push-pull center tap is unlimited and the voltage at that point ( $V_{ct}$ ) remains high. The core then moves further into saturation, where its impedance eventually vanishes and transistor currents increase drastically. With high current and voltage, the transistors will fail.

With the high impedance looking back into the dot end of  $N_{LP}$  as shown in Figure 5.19, however, as the push-pull core moves into saturation drawing more current, the high current causes a voltage drop at  $V_{ct}$ . This reduces the volt-second product on the half primary, which is moving toward saturation, and prevents complete core saturation.

Thus the high source impedance of  $N_{LP}$  does not fully prevent core saturation. In the worst case, it keeps the core close to the knee of the  $BH$  loop, which is sufficient to keep transistor currents from rising to disastrous levels. The major drawback of push-pull circuit flux imbalance is thus not a problem with this inverter.

#### 5.6.7.2 Decreased Push-Pull Transistor Current in Flyback Current-Fed Topology

In a conventional pulse-width-modulated push-pull, driven at the center tap from a low-impedance voltage source, it is essential to avoid simultaneous conduction in the transistors by providing a dead time of about 20% of a half period between turn “off” of one transistor and turn “on” of the other. This results in higher peak transistor current for the same output power, since output power is proportional to average transistor current.

This dead time is essential in the voltage-fed push-pull, for if  $Q1$ ,  $Q2$  were simultaneously “on,” the half primaries could not sustain voltage. Then, the transistor collectors would rise to the supply voltage, which would remain high, and with high voltage and high current, the transistors would fail.

In the current-fed circuit, there is no problem if both transistors are simultaneously “on” under transient or fault conditions, when the DC input voltage is momentarily lower than specified or with storage times greater than specified, because of the high impedance looking back into the dot end of  $N_{LP}$ . Should both transistors turn “on” briefly